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(54) Decoder for a compressed digital video signal using a common memory for decoding and 2/3 pull-down conversion.

(57) An appartaus for expanding a compressed digital video signal is disclosed representing a motion picture to provide a digital video output signal. The compressed digital video signal comprises plural interlaced frames and has a frame rate of 24 Hz, the digital video output signal comprises plural pictures and has a picture rate of at least 49 Hz. The apparatus comprises a frame memory (45) comprising no more than four pages, each page storing one frame, expander means for expanding each frame of the compressed digital video signal to derive a reconstructed interlaced frame and control means (68). The control means (68) operates by writing of each reconstructed interlaced frame into one page of the frame memory (45) and reading out of the reconstructed interlaced frames stored in the pages of the frame memory (45) to provide the pictures of the digital video output signal. The reading out is controlled to effect 2-3 pull down conversion of the reconstructed interlaced frames stored in the pages of the frame memory (45) with a frame rate of 24 Hz to provide the pictures of the digital video output signal with a picture rate of at least 49 Hz.

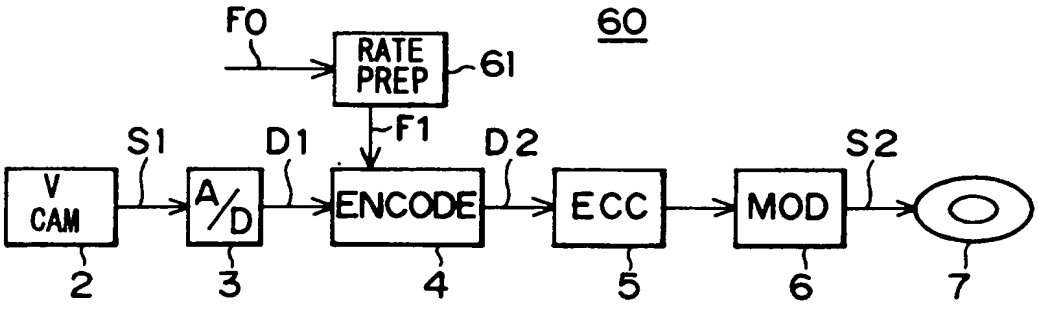

FIG. 6

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Field of the Invention

This invention relates to an apparatus for decoding a compressed interlaced digital video signal having frame rate of 24 Hz to provide a digital output signal that is either interlaced with a field rate of 60 Hz or is non-interlaced with a frame rate of 60 Hz and in which a single field memory having four pages, each storing one frame, is used for the decoding and for picture rate conversion.

Background of the Invention

Since a very large amount of data is required to represent a motion picture digitally, the digital video signal representing the motion picture is conventionally compressed using a high-efficiency compression process to enable the digital video signal to be transmitted, distributed, or stored using significantly less data. Figures 1 and 2 respectively show the construction of a known recording apparatus for recording a digital video signal representing a motion picture and of a known reproducing apparatus for reproducing a compressed digital video signal in which the digital video signal is compressed before recording, and the compressed digital video signal is expanded after reproduction.

Specifically, in the recording apparatus 1 shown in Figure 1 for recording a digital video signal, the analog video signal S1 from a video signal source, such as the video camera (VID CAM) 2, is converted into a digital video signal by the analog-to-digital converter (A/D) 3. The resulting digital video signal D1 is fed into the encoder (ENCODE) 4. where it is compressed. The error correction circuit (ECC) 5 adds error correcting codes to the compressed digital video signal D2 from the encoder 4, and the modulation circuit (MOD) 6 modulates the resulting signal using a predetermined modulating method. The recording signal S2 from the modulation circuit is recorded on the recording medium 7, which is, for example, an optical disk.

In the reproducing apparatus 8 shown in Figure 2 for reproducing a compressed digital video signal, the signal S3 reproduced from the recording medium 7 is demodulated by the demodulation circuit (DEMOD) 9. The error correcting circuit (ECC) 10 subjects the demodulated signal to error detection and correction to produce the compressed digital video signal D3. The decoder (DECODE) 11 expands the compressed digital video signal D3 from the error correction circuit 10 to produce the digital output signal D4. The digital-to-analog converter (D/A) 12 converts the digital output signal D4 to an analog signal for delivery as the analog video signal S4 to the monitor (TV MONI) 13 or the like for display. Alternatively, the digital output signal D4 can be delivered to the monitor 13 directly.

Figure 3 shows the construction of the encoder 4 of the recording apparatus 1 in detail. The encoder 4 receives the digital video signal D1 and stores it in the frame memory (FRM MEM) 20, which consists of a random-access memory (RAM). The digital video signal is read out from the frame memory 20 at a predetermined timing and is fed to the subtractor 22 and one pole of the switch 32. The other pole of the switch 32 is connected to the output of the subtractor 22. The wiper of the switch 32 is connected via the block dividing circuit 21 and the subtractor 22 to the orthogonal transform circuit 23, which is, for example, a discrete cosine transform (DCT) circuit. Depending on the state of the switch 32, the orthogonal transform circuit 23 orthogonally transforms a block of the digital video signal D1 or a block of differences between a block of the digital video signal and a corresponding reference block. The orthogonally transform circuit applies, for example, a discrete cosine transform (DCT). The resulting transform coefficients are quantized by the quantizing circuit (Q) 24. The variable length coding circuit (VLC) 25 codes the quantized transform coefficients using variable length coding such as Huffman coding. The resulting digital video data D0 are fed to the video output buffer 26, where they are temporarily stored.

Each picture (i.e., each frame or each field) of the digital video signal may be coded using intra-picture coding or inter-picture coding. A picture coded using intra-picture coding (called an I-picture) is coded by itself, without reference to any other picture. When a picture is coded as an I-picture, the switch 32 feeds each picture block of the picture directly to the orthogonal transform circuit 23.

A picture coded using inter-picture coding (called a P-picture or a B-picture) is coded with reference to a reference picture, which is derived from one or more previous or following pictures. When a picture is coded using inter-picture coding, the subtractor 22 generates blocks of differences between blocks of the picture and corresponding blocks of the reference picture, and passes each block of differences via the switch 32 to the orthogonal transform circuit 23 for coding.

The reference picture with respect to which the picture is coded is derived from reconstructed I-pictures and P-pictures stored in the frame memory 20 as follows: a P-picture is coded with forward prediction using as its reference picture a temporally preceding I-picture or P-picture. A B-picture is coded with bi-directional prediction using as its reference picture one of the following three types of pictures: a temporally preceding I-picture or P-picture; a temporally following I-picture or P-picture; or a picture formed by interpolation between a temporally-preceding I-picture or P-picture and a temporally-following I-picture or P-picture.

The reconstruction of the reconstructed I-pic-

tures and P-pictures stored in the frame memory 20 will now be described. The block of quantized transform coefficients derived from each block of each I-picture or each P-picture is fed from the quantizing circuit 24 to the local decoder 33. The local decoder is constituted by the inverse quantizer 27, the inverse orthogonal transform circuit 28, and the adder 29. The local decoder 33 decodes each block of quantized transform coefficients to provide a block of a reconstructed picture. The block of the reconstructed picture is then stored in the frame memory 20.

In the local decoder 33, each block of quantized transform coefficients passes from the quantizer 24 to the inverse quantizing circuit (IQ) 27, where it is inversely quantized. Each resulting block of transform coefficients is fed into the inverse orthogonal transform circuit (IDCT) 28, where it is subject to an inverse orthogonal transform, such as an inverse DCT. Each resulting locally-decoded block from the inverse orthogonal transform circuit 28 is supplied to the adder 29, where it is added to its corresponding reference block from the motion compensator 31. The resulting reconstructed picture block is fed into the frame memory 20, where it is stored as a block of a reconstructed picture stored in the memory. When the picture being coded is an I-picture, the motion compensator 31 supplies no reference block to the adder 29, and the reconstructed picture block is derived solely from the locally-decoded block from the inverse orthogonal transform circuit 28.

By the process just described, a reconstructed picture is derived from each I-picture and each P-picture by decoding compressed digital data that is identical to the compressed digital data supplied via the VLC circuit 25 to the video output buffer 26. The reconstituted picture is written into the frame memory 20. The resulting reconstructed pictures stored in the frame memory 20 are then used in coding P-pictures and B-pictures.

When the current picture is coded using inter-picture coding (i.e., is a P-picture or a B-picture), the reference block for coding each block of the picture is generated by the motion compensator 31 in response to the motion detector 30. The motion detector 30 performs block matching between each block of the current picture and the reference picture derived from the reconstructed pictures stored in the frame memory 20. This detects the motion of each block of the current picture relative to the reference picture. The motion detector 30 generates a motion vector representing this motion, and feeds the motion vector to the VLC circuit 25 and to the motion compensator 31. The VLC circuit 25 applies variable-length coding to the motion vector and combines the result with the variable-length coded transform coefficients received from the quantizer 24. The VLC circuit 25 feeds the resulting digital video data to the video output buffer 26.

In response to the motion vector received from the motion detector 30, the motion compensator 31 carries out motion compensation on the reference picture derived from the reconstructed pictures stored in the frame memory 20, and provides the resulting reference block corresponding to the picture block of the current picture to the subtractor 22 and to the adder 29. As described above, the subtractor 22 subtracts the reference block from the motion compensator 31 from the picture block of the current picture to derive a block of differences for coding, and the adder 29 adds the reference block from the motion compensator 31 to the locally-decoded block from the inverse orthogonal transform circuit 28 to generate a block of the reconstructed picture, which it supplies to the frame memory 20 for storage.

The video output buffer 26 monitors the number of bytes of compressed digital video data accumulated therein and adjusts quantizing step size in the quantizing circuit 24 so that the accumulated number of bytes of compressed digital data does not cause the video output buffer to overflow or to underflow. The compressed digital video data stored in the video output buffer 26 is read out at a constant rate, and is delivered to the error correction circuit 5 as the compressed digital video signal D2.

The decoder 11 of the motion picture reproducing apparatus 8 (Figure 2) is constructed as shown in Figure 4. The compressed digital video signal D3 is transferred at a constant transfer rate from the error correction circuit (ECC) 10 to the video input buffer 40, where it is stored. The compressed digital video data for each picture is read out from the video input buffer 40, and is supplied to the inverse VLC circuit 41. The inverse variable length coding circuit (inverse VLC circuit) applies inverse VLC coding to the compressed digital data for each picture, and supplies the resulting blocks of quantized transform coefficients to the inverse quantizing circuit (IQ) 42.

After it has finished applying inverse VLC coding to the compressed digital data for each picture, the inverse VLC circuit 41 feeds a request code RQ to the video input buffer 40 to cause the video input buffer to provide the compressed digital data for the next picture. In response to the request code, the video input buffer 40 transfers the compressed digital video data of the next picture to the inverse VLC circuit 41. The transfer rate of this process is the same value as the transfer rate from the VLC circuit 25 to the video output buffer 26 in the encoder 4 (Figure 3), so the video input buffer 40 will neither overflow nor underflow when it receives compressed video data at a constant transfer rate from the storage medium 7. In fact, in the encoder 4, the video output buffer 26 controls the number of bytes of compressed video data accumulated therein by emulating the video input buffer 40 in the decoder 11 such that the video input buffer will neither overflow nor underflow.

In addition to applying inverse VLC coding to the compressed digital data for each picture, the inverse VLC circuit 41 extracts from the compressed digital data the motion vector MV for each block and quantizing step size data SS. The quantizing step size data is generated by the encoder 4 (Figure 1) and is included in the recording signal recorded on the recording medium 7 for use in dequantizing the quantized transform coefficients in the dequantizer 42 in the decoder 11. The motion vector MV is generated by the motion detector 30 (Figure 3), and is included in the recording signal recorded on the recording medium 7 for use in the motion compensator 46 in the decoder 11.

The dequantizer 42 dequantizes each block of quantized transform coefficients supplied by the inverse VLC circuit 41 in accordance with quantizing step size data SS extracted from the compressed digital video data by the inverse VLC circuit 41, and supplies each resulting block of transform coefficients to the inverse orthogonal transform (IDCT) circuit 43.

The inverse orthogonal transform circuit 43 applies an inverse orthogonal transform, such as an inverse discrete cosine transform, to each block of transform coefficients supplied by the dequantizing circuit 42 to provide a decoded block. The decoded block is supplied to the adder 44, which also receives the corresponding reference block of the corresponding reference picture derived by the motion compensator 46 from one or more of the reconstructed pictures stored in the frame memory 45. The resulting reconstructed picture block from the adder 44 is stored in the frame memory 45 as a block of a new reconstructed picture.

If the current picture is an I-picture, the motion compensator 46 provides no reference block to the adder 44, and the reconstructed block is generated using the decoded block alone. If the current picture is a P-picture, having an I-picture or another P-picture as its reference picture, the I-picture or P-picture is copied from the frame memory 45 to the motion compensator 46 as the reference picture for the current picture. The motion compensator 46 applies motion compensation to the reference picture copied from the frame memory 45 in accordance with the motion vector for the current block of the current picture. The motion compensator 46 then provides the resulting block of the reference picture to the adder 44 as the reference block for the current block of the current picture.

The adder 44 adds the decoded block from the inverse orthogonal transform circuit 43 to the reference block from the motion compensator 46 to reconstruct the current block of the current P-picture, which is stored in the frame memory 45. This process is then repeated for the remaining blocks of the current P-picture until all of the blocks of the current picture have been reconstructed.

If the current picture is a B-picture, the one or more I-pictures and/or P-pictures are copied from the frame memory 45 to the motion compensator 46, which generates from these pictures, in response to the motion vector for the current block, the reference block for reconstructing the current block. The motion compensator 46 supplies the reference block to the adder 44.

The adder 44 adds the decoded block from the inverse orthogonal transform circuit 43 to the reference block from the motion compensator 46 to reconstruct the current block of the current B-picture, which is stored in the frame memory 45. This process is then repeated for the remaining blocks of the current B-picture until all of the blocks of the current picture have been reconstructed.

The current picture stored in the frame memory 45 as just described is read out in line scan order by the scanning address generating circuit (FOSL) 47 addressing the frame memory 45. The resulting digital output signal D4 is then fed to the monitor 13 (Figure 2), either directly, or via the digital-to-analog converter 12. After it has been read out, the current picture, if an I-picture or P-picture, is briefly stored in the frame memory 45 for use in decoding other P- and B-pictures.

In the manner just described, the recording apparatus and the reproducing apparatus reduce the redundancy within each picture by orthogonally transforming square blocks of the picture, and reduce the redundancy between pictures by means of the motion vector and block matching. These two techniques are combined to compress the digital video signal representing the motion picture so that the motion picture may be recorded, transmitted, or distributed using a relatively small amount of data.

A picture rate conversion method known as 2-3 pull-down conversion is used when an interlaced video signal having a field rate of 60 Hz is derived from a motion picture film source, such as a motion picture film, or a 24-frame video signal, by means of a telecine or other apparatus. This method must be used because the interlaced video signal has a picture rate of 60 Hz, i.e., a field rate of 60 Hz, whereas the motion picture film source has a picture rate of 24 Hz, i.e., a frame rate of 24 Hz. In this method, for example as shown in Figures 5A and 5B, two fields of the video signal are derived from the first of each two consecutive frames of the motion picture film source, and three fields of the video signal are derived from the second of the two fields of the motion picture film source.

In Figures 5A and 5B, Figure 5A shows four consecutive frames, including the frames 50 and 51, of a motion picture film source having a frame frequency of 24 Hz. Each frame of the motion picture film source is scanned twice to provide an odd field, indicated by solid lines, and an even field, indicated by

broken lines, offset from the odd field by one line.

Accordingly, the first two fields of the interlaced video signal are derived from the zero-th motion picture film source frame 50. The odd field produced by scanning the motion picture film source frame 50 provides the zero-th field 52, and the even field produced by scanning the motion picture film source frame 50 provides the first field 53 of the interlaced video signal.

The next three fields of the interlaced video signal are derived from the first motion picture film source frame 51. The odd field produced by scanning the motion picture film source frame 51 provides the second field 54, and the even field produced by scanning the motion picture film source frame 51 provides the third field 55 of the interlaced video signal. Then, the motion picture film source frame 51 is scanned a second time to provide an odd field as the fourth field 56 of the interlaced video signal. The process is repeated with the third frame 57 and the fourth frame 58 of the motion picture film source, except that repeated field is the even field 59, as shown. Note that the interlaced video signal frame consisting of the fourth and fifth fields, and the interlaced video signal frame consisting of the sixth and seventh fields are each derived from two different frames of the motion picture film source.

Thus, although the frame frequency of the motion picture film source is different from the field frequency of the interlaced video signal, the frequencies are made to match by scanning every other frame to generate an additional field. This is the basic principle of the 2-3 pull-down conversion method. The 2-3 pull-down conversion method generates an interlaced video signal in which certain fields, such as the second field 54 and the fourth field 56, are completely identical to one another.

A 2-3 pull-down conversion technique similar to that just described is used when an interlaced video signal having a field rate of 50 Hz is derived from a motion picture film source having a frame rate of 24 Hz. PAL-system and SECAM-system video signals are examples of interlaced video signals with a field rate of 50 Hz. When an interlaced video signal with a field rate of 50 Hz is generated from a motion picture film source with a frame rate of 24 Hz, three fields of the interlaced video signal are derived from every twelfth frame of the motion picture film source, and two fields of the interlaced video signal are derived from all other frames.

In the following description, it will be understood that references to video signals with a picture rate (i.e., field rate or frame rate) of 60 Hz also refer to video signals having a picture rate of 50 Hz, and that references to 2-3 pull down conversion in which a video signal having a picture rate of 60 Hz is derived from a motion picture film source or a compressed video signal with a frame rate of 24 Hz also refer to 2-3 pull down conversion in which a video signal with a picture rate of 50 Hz is derived from a motion picture film source or a compressed video signal with a frame rate of 24 Hz. It is also to be understood that references to picture rates of 24 Hz, 50 Hz. and 60 Hz also encompass corresponding non-integer picture rates.

Because an interlaced video signal generated by 2-3 pull-down conversion includes duplicate fields, some types of apparatus for compressing a digital video signal representing a motion picture detect the duplicate fields in the interlaced video signal having a field rate of 60 Hz. Such types of apparatus perform field rate conversion by removing one of each pair of duplicate fields, and compress the resulting digital video signal in interlaced frames having a frame rate of 24 Hz. This improves the overall efficiency of the compression process. Moreover, to further increase the efficiency of the compression process, the interlaced frames may be compressed either in field mode or in frame mode.

To expand a digital video signal compressed in the way just described, the decoder expands the compressed digital video signal to provide an interlaced digital video signal with a frame rate of 24 Hz. The decoder then performs 2-3 pull down conversion to obtain an interlaced video signal with a field rate of 60 Hz.

If such a decoder is adapted to expand the compressed digital video signal in the manner described to provide a non-interlaced output signal for display on a non-interlaced monitor, such as on a non-interlaced computer monitor, the output signal will be displayed with a high picture quality, close to that of the original motion picture film source with the frame rate of 24 Hz. However, to adapt the decoder to convert the interlaced pictures obtained by expanding the compressed digital video signal into a non-interlaced video signal requires a field rate conversion circuit or the like, which increases the complexity of the decoder.

Objects and Summary of the Invention

In view of the foregoing, an object of this invention is to provide a decoder for expanding a compressed digital video signal representing a motion picture. The decoder has a simplified construction, and expands a compressed digital video signal representing a motion picture in frames having a frame rate of 24 Hz, provides 2-3 pull down conversion, to provide an interlaced or a non-interlaced output signal.

Accordingly, the invention provides an apparatus for expanding a compressed digital video signal representing a motion picture to provide a digital output signal. The compressed digital signal comprises plural interlaced frames having a frame rate of 24 Hz. The digital output signal comprises plural pictures

having a picture rate of at least 49 Hz. The apparatus comprises a frame memory comprising no more than four pages, each page storing one frame. The apparatus also includes an expander for expanding the compressed digital signal to provide a reconstructed interlaced frame from each frame of the compressed digital video signal. Finally, the apparatus includes a controller that controls writing of each reconstructed interlaced frame into one page of the frame memory, and reading of the reconstructed interlaced frames stored in the four pages of the frame memory to provide pictures of the digital output signal. Reading is controlled to effect 2-3 pull down conversion of the reconstructed interlaced frames stored in the frame memory with a frame rate of 24 Hz to provide the pictures of the digital output signal with a picture rate of at least 49 Hz.

The invention further provides a system for recording a digital video input signal representing a motion picture to provide a compressed digital video signal comprising plural interlaced frames having a frame rate of 24 Hz, and for expanding the compressed digital video signal to provide a digital video output signal comprising plural pictures having a picture rate of at least 49 Hz. The system comprises a compressor and an expander.

The compressor includes a system for deriving from a motion picture film source a non-interlaced digital video signal comprising plural frames having a frame rate of 24 Hz, and a circuit for performing 2-3 pull-down conversion on the non-interlaced digital video signal to derive an interlaced digital video signal having a frame rate of greater than 24 Hz. A circuit compresses the interlaced digital video signal to provide a compressed digital video signal with a frame rate of greater than 24 Hz. Finally, a circuit reduces the frame rate of the compressed digital video signal with a frame rate of greater than 24 Hz to 24 Hz to provide the compressed digital video signal.

The expander includes a frame memory comprising no more than four pages, each page storing one frame. The apparatus also includes an expander for expanding the compressed digital signal to provide a reconstructed interlaced frame from each frame of the compressed digital video signal. Finally, the apparatus includes a controller that controls writing of each reconstructed interlaced frame into one page of the frame memory, and reading of the reconstructed interlaced frames stored in the four pages of the frame memory to provide pictures of the digital output signal. Reading is controlled to effect 2-3 pull down conversion of the reconstructed interlaced frames stored in the frame memory with a frame rate of 24 Hz to provide the pictures of the digital output signal with a picture rate of at least 49 Hz.

The nature, principle and utility of the invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings in which like parts are designated by like reference numerals or characters.

Brief Description of the Drawings

Figure 1 is a block diagram showing the construction of a conventional apparatus for compressing and recording a digital video signal, such as a digital video signal representing a motion picture.

Figure 2 is a block diagram showing the construction of a conventional apparatus for reproducing and expanding a compressed digital video signal.

Figure 3 is a block diagram showing the construction of the encoder of the conventional compressing and recording apparatus shown in Figure 1.

Figure 4 is a block diagram showing the construction of the decoder in the conventional reproducing and expanding apparatus shown in Figure 2.

Figures 5A and 5B are schematic diagrams explaining the theory of 2-3 pull down conversion.

Figure 6 is a block diagram showing an apparatus for providing the compressed digital video signal for expansion by the reproducing and expanding apparatus incorporating the expander according to the invention.

Figure 7 is a block diagram showing the reproducing and expanding apparatus including the expander according to the invention.

Figure 8 is a block diagram showing the circuit structure of the expander according to the invention.

Figures 9A and 9B schematically show the relationship between interlaced scanning and non-interlaced scanning.

Figures 10A and 10B schematically illustrate the combination of 2-3 pull down conversion and non-interlaced scanning.

Figure 11 is a schematic diagram showing the concept of the process by which reconstructed interlaced frames derived from the compressed video signal are written into the pages of the frame memory and are read out to provide the frames of the interlaced digital output signal.

Figure 12 is a schematic diagram showing the concept of the process by which reconstructed interlaced frames derived from the compressed video signal are written into the pages of the frame memory and are read out to provide the frames of the non-interlaced digital output signal.

Figure 13 is a block diagram schematically showing the construction of the rate converter in the expander according to the invention.

Figure 14 is a connection diagram showing the construction of the first converter in the rate converter in the expander according to the invention.

Figure 15 is a connection diagram showing the construction of the second converter in the rate converter in the expander according to the invention.

Figure 16 is a schematic diagram explaining the

operation in the non-interlaced mode of the rate converter in the expander according to the invention.

Figures 17A to 17K are timing charts explaining an operation in the non-interlaced mode of the rate converter in the expander according to the invention.

Figure 18 is a schematic diagram explaining the operation in the interlaced mode of the rate converter in the expander according to the invention.

Detailed Description of the Invention

Preferred embodiments of the invention will be described with reference to the drawings.

Referring to Figure 6, in which components corresponding to those in Figure 1 are denoted by the same reference numerals, the recording apparatus 60 includes the encoder on which premises the present invention is based. In the recording apparatus, instead of the video signal S1 being received from the video camera 2, the digital interlaced video signal F0 having a field rate of 60 Hz, derived from a motion picture film source by 2-3 pull down conversion, is fed into the video input terminal of the field rate preprocessing section 61.

The rate preprocessing section 61, converts the digital interlaced video signal F0 with a field rate of 60 Hz into the frames of an interlaced video signal F1 with a frame rate of 24 Hz. The interlaced video signal F1 is encoded by the encoder 4 in a manner similar to that described above with reference to the conventional encoder. After the error correction circuit (ECC) 5 had added error correction codes in a similar manner to that described above with reference to the conventional decoder, the resulting compressed digital video signal D2 is modulated according to a predetermined modulation method by the modulation circuit 6. The resulting recording signal S2 is recorded on the recording medium 7, which is, for example, an optical disk.

In Figure 7, in which components corresponding to those shown in Figure 2 are denoted by the same reference numerals, the reproducing apparatus 65 includes the decoder according to the present invention. In Figure 7, the signal S3, obtained by reproducing the recording signal from the recording medium 7, is demodulated by the demodulation circuit 9, and error detection and correction is applied by the error correction circuit 10. The resulting compressed digital video signal D3 is fed into to the decoder 11. The decoder 11 produces an interlaced digital video signal having a frame rate of 24 Hz.

In the decoder 11, the rate converter 66 controls the timing of writing to and reading from a frame memory in the decoder in synchronization with the decoding to perform 2-3 pull down conversion, and, optionally to convert the digital output signal read out of the frame memory to an interlaced signal with a frame rate of 30 Hz to a non-interlaced signal with a double-speed frame rate of 60 Hz. The analog-to-digital converter 12 converts the digital video signal produced by the decoder 11 into an analog video signal for delivery to the monitor 13 as the video output signal S4. Alternatively, the digital video signal D4 may be delivered directly to the monitor 13 as the video output signal if the monitor can operate with a digital input signal. The scanning format of the video output signal is set according to a interlace/non-interlace control signal. The control signal can be entered into the decoder 11 by the user operating a control on the decoder, or the control signal can be provided by feeding information indicating whether the monitor 13 is capable of non-interlaced scanning with a frame rate of 60 Hz from the monitor 13 to the decoder 11 via a suitable signal path (not shown).

In the motion picture reproducing apparatus 65, the decoder 11 is constructed as shown in Figure 8, in which components corresponding to those in the decoder shown in Figure 4 are indicated by the same reference numerals. In Figure 8, the frame memory 45 is constructed with four pages of random access memory (RAM), each storing one frame of the reconstructed digital video signal. The bus scheduler 67 controls access to the pages of the frame memory 45.

The invention relates to how the writing and reading of video pictures reconstructed using a conventional decoding procedure into and out of the pages of the frame memory 45 are controlled. In the conventional decoding procedure used in the decoder according to the invention, inverse VLC processing is applied to the reproduced compressed digital video signal; after which an inverse orthogonal transform, such as an inverse DCT, including inverse quantizing is performed; and, finally. motion compensation is performed by adding each locally-decoded block from the inverse orthogonal transform to a block of a reference picture selected from the frame memory 45.

In the decoder 11, the rate converter 66 for effecting frame rate conversion of 24 Hz to 60 Hz or 24 Hz to 30 Hz provides information to the bus scheduler 67 to indicate the page of the frame memory 45 from which reading is to take place, and into which writing is to take place, and the timing of such reading and writing.

In practice, when the reconstructed stored in the frame memory 45 are read out to provide the digital output signal, the processing to derive a non-interlaced digital output signal from the interlaced pictures stored in the frame memory is as follows. To generate the non-interlaced digital output signal, the line frequency (horizontal frequency) of the stored interlaced pictures is doubled to provide a frame with double the number of scanning lines of each field of the interlaced signal, while the frame frequency of the non-interlaced signal is made the same as field fre-

quency (vertical frequency) of the interlaced signal. As shown in Figures 9A and 9B, the vertical resolution of the frames of the non-interlaced signal (Figure 9B) is improved compared with the vertical resolution of each field of the interlaced signal (Figure 9A).

The result of combining scan conversion processing with 2-3 pull down conversion is shown in Figures 10A and 10B, in which the odd field of a regenerated interlaced frame, such as the frame 80, indicated by broken lines in Figure 10A, is first written into part of page of the frame memory 45. Then, the even field of the interlaced frame 80, indicated by solid lines in Figure 10A is written into the same page of the frame memory. The interlaced frame 81 is also written in to one page of the frame memory 45.

The interlaced frames 80 and 81 stored in the pages of the frame memory 45 as just described are read out as frames of a non-interlaced digital output signal as follows. When the frame 80 is read, the lines of the odd field, indicated by the broken lines in Figure 10B, are read alternately with the lines of the even field, indicated by the solid lines in Figure 10B, twice at double speed to provide the frames 82 and 83 of the non-interlaced digital output signal. Each frame is read in 1/60 sec. Then the frame 81 is read out of its page from the frame memory 45. To provide the required 2-3 pull-down conversion, the odd field lines and the even field lines of the frame 81 are alternately read three times to provide the frames 84, 85, and 86 of the digital output signal. Each of frames 82 through 86 is read in 1/60 sec.

Accordingly, to provide a non-interlaced digital output signal, each frame stored in a page of the frame memory 45 is read out at least twice at a frame frequency of 60 Hz. Alternatively, each frame can be read once from the frame memory 45 and the resulting frame stored in another frame memory whence the frame is read a second time and/or a third time. However, this method requires an additional frame memory. Consequently, in this embodiment of the invention, each frame is read at least twice from the frame memory 45, with a frequency of 60 Hz.

Figures 11 and 12 show conceptually the reading and writing process according to the invention using, for example, the I-picture, B-picture, and P-picture picture types standardized by the Motion Picture Experts Group (MPEG) method of encoding of a motion picture for storage. Figures 16 and 18 show the reading and writing process with the timing and multiple reading required to implement 2-3 pull-down conversion to provide a digital output signal with a frame rate of 30 Hz or 60 Hz.

Each frame of the digital video signal may be coded using intra-picture coding or inter-picture coding. An I-picture is a frame coded using intra-picture coding. in which the picture is coded without reference to a previous or a following picture. A P-picture or a B-picture is coded with reference to a reference picture, which is derived from one or more reconstructed previous or following pictures. When a picture is coded using inter-picture coding, the picture may be coded with reference to a reference picture as follows: a P-picture is coded with forward prediction using as its reference picture a temporally preceding I-picture or P-picture. AB-picture is coded with bi-directional prediction using as its reference picture one of the following three types of pictures: a temporally preceding I-picture or P-picture; a temporally following I-picture or P-picture; or a picture formed by interpolation between a temporally-preceding I-picture or P-picture and a temporally-following I-picture or P-picture.

Figure 11 shows decoded pictures written into the pages of the frame memory 45 in the order of, for example, I-picture, B-picture, B-picture, P-picture, B-picture, B-picture, P-picture, B-picture, B-picture, P-picture, ..., as indicated by the solid lines labelled I0, B1, B2, P3, B4, B5, P6, B7, B8, P9, ... respectively. The pictures are read from respective pages of the frame memory 45 to provide the digital output signal in the order in which they are to be displayed, i.e., in the order of B1, B2, I0, B4, B5, P3, B7, B8, P6, B10, B11, P9, ...

In Figure 11, the four pages of the frame memory 45 into which the frames of the reconstructed pictures can be written are indicated by M0, M1, M2, and M3. The page of the frame memory into which each of the frames in the sequence set forth above is written is indicated in Figure 11 by the one of the four rows marked M0 through M3 on which the frame number appears. For example, frame I0 appears on the line marked M0, thus the frame I0 is written into page M0 of the frame memory 45. In addition, each page of the frame memory 45 is divided into an even field portion fe and an odd-field portion fo, also shown in Figure 11 into which the odd field and the even field, respectively, of the frame is written. Finally, an axis showing the relationship between writing time and reading time is displayed at the top of Figure 11. This axis is not a real time axis.

In the writing and reading sequence shown in Figure 11, the I-picture I0, indicated by the solid arrow I0, is first written in page M0 of the frame memory 45. Next, the B-picture B1, indicated by the solid arrow B1, is written into page M2 of the frame memory 45; and the following B-picture B2, indicated by the solid arrow B2, is written into page M3 of the frame memory 45. At the same time, the B-picture B1, indicated by the broken arrow B1, is read out from page M2.

Next, the P-picture P3, indicated by the solid arrow P3, is written into page M1 of the frame memory 45, and, at the same time, the B-picture B2, indicated by the broken arrow B2, is read out from the page M3 of the frame memory 45. The B-picture B4, indicated by the solid arrow B4, is written into page M2 of the frame memory 45, and, at the same time, the I-picture I0, indicated by the broken arrow I0, is read out

from the page M0 of the frame memory 45. By process of writing and reading similar to that just described, the remaining pictures in the picture sequence are processed.

In the decoding apparatus according to the invention, the frame memory 45 is constructed with four pages, each storing one frame. Separate pages are designated for storing I-pictures and P-pictures and for storing B-pictures. Only I-pictures and P-pictures are stored in pages M0 and M1 of the frame memory 45; and only B-pictures are stored in pages M2 and M3 of the frame memory 45. Accordingly, when 2-3 pull down conversion is not to be performed, since a page corresponding to each of four frames is provided in the frame memory 45, pictures having both a field structure and a frame structure may be written and read with timings similar to those shown in Figure 11. This is done by delaying the start of reading from each page of the frame memory by a time corresponding to one frame from the start of writing to the page of the memory. This provides sufficient time, even when an interlaced signal is being generated.

Providing the frame memory 45 with four pages, each storing one frame, simplifies controlling the memory because, as shown in Figure 12, reading out from the frame memory to provide a non-interlaced digital output signal can be done in a manner similar to that for reading out from the frame memory to provide an interlaced digital output signal.

Figure 12 shows the conceptually the reading and writing sequence for reading out an interlaced digital output signal from the frame memory 45. In Figure 12, the I-picture I0, indicated by the solid arrow I0, is first written into page MO of the frame memory 45. Next, the B-picture B1, indicated by the solid arrow B1, is written into page M2 of the frame memory 45; and the following B-picture B2, indicated by the solid arrow B2, is written into page M3 of the frame memory 45. At the same time, the B-picture B1 is read out twice from page M2 of the frame memory 45, as indicated by the four broken arrows B1. The lines of the odd field and of the even field stored in the page M2 are alternately read out to provide one frame of the digital output signal. Then, the of the odd field and of the even field stored in the page M2 are alternately read a second time to provide the next frame of the digital output signal.

Next, the P-picture indicated P3, by the solid arrow P3, is written into page M1 of the frame memory 45. At the same time, the B-picture B2 is read out twice from page M3 of the frame memory 45, as indicated by the four broken arrows B2. The lines of the odd field and of the even field stored in the page M1 are alternately read out to provide one frame of the digital output signal. Then, the of the odd field and of the even field stored in the page M1 are alternately read a second time to provide the next frame of the digital output signal.

Next, the B-picture B4, indicated by the solid arrow B4, is written into page M2 of the frame memory 45, and, at the same time, the I-picture I0 is read out twice from page M0 of the frame memory 45, as indicated by the four broken arrows I0. The lines of the odd field and of the even field stored in the page M0 are alternately read out to provide one frame of the digital output signal. Then, the of the odd field and of the even field stored in the page M0 are alternately read a second time to provide the next frame of the digital output signal.

In the decoder according to the invention, the rate converter 66 is constructed as shown in Figure 13. The rate converter 66 includes the first converters 90A, 90B, 90C, and 90D, which perform 2-3 pull down conversion by designating, via the bus scheduler 67 the page of the frame memory 45 into which each reconstructed picture is to be written and from which each frame of the digital output signal is to be read. The rate converter also includes the second converters 91A, 91B, 91C, and 91D which control the timing of the writing and reading operations.

The construction of each of the first converters 90A, 90B, 90C, and 90D is shown in detail in Figure 14, and that of each of the second converters 91A, 91B, 91C. and 91D is shown in detail in Figure 15. The converters are constructed from logic gates and flip-flops. The first converters each include the frame counters 100 and 103, the decoder 101, the latches 102, 104, 105, 106, 109, and 110, and the clock counters 107 and 108, etc. One first converter and one second converter is provided for each page of the frame memory 45. In the example shown in Figure 13, four pairs of converters are provided for the 4-page frame memory 45.

Each of the first converters 90A, 90B, 90C, and 90D is initialized by the MPEG group of pictures (GOP) start code, and determines the picture type of each picture by recognizing the MPEG picture start code (PSC).

Circuit operation of the first converter 90B and of the second converter 91B controlling writing to and reading from the page M1 of the frame memory 45 will be described with reference to Figures 14. 15, and 17A through 17K. The construction of the first converters 90A, 90C and 90D, and the second converters 91A, 91C and 91D is the same. The first converters 90A. 90B, 90C, and 90D and the second converters 91A, 91B, 91C, and 91D respectively operate on the memory pages M0, M1, M2, and M3 shown in the lower part of Figure 16. It should be noted that signal names in the circuit diagrams of Figures 14 and 15 correspond to those in Figures 17A through 17K.

Specifically, the first B-picture B1 in the GOP is written into page M2 of the frame memory 45 when the write enable signal W_{EN}- (the "-" in W_{EN}- and in similar designations in the following description indi-

cates the negative and corresponds to the bar in the Figures) of the second converter 91 is active (i.e., is at a low level), as shown in Figure 17C. While the first B-picture B1 is being written, the signal W_{B_END} from the latch 108 remains low and inhibits the frame counters 100 and 103.

When writing the first the B-picture B1 is finished, the signal W_{B_END} from the latch 108 goes high in response to W_{B}-, as shown in Figures 17E and 17F, which enables the frame counters 100 and 103. The frame counter 100 counts the frames read out of the frame memory 45 at a frame rate of 60 Hz, and the decoder 101 decodes the output of the counter 100 to generate the 2/3- signal, as shown in Figure 17J.

The 2/3- signal is inverted by the inverter 130 and fed into the latch 102, together with the 27 MHz clock signal to generate the trigger pulse 2/3 -tr shown in Figure 17K. The 2/3-tr trigger pulse starts the counter 103, the output of which is R_{B}- (Figure 17H), which is inverted by the inverter 131 to produce R_{IorP}- (Figure 17G). The signals R_{B}- and R_{IorP}- are the read enable signal for a B-picture and the read enable signal for an I-picture or a P-picture, respectively.

The two read enable signals R_{B}- and R_{IorP}- are latched by the latches 104 and 105, respectively, the outputs of which are fed into the OR-gate 132. The output of the OR-gate is fed into one input of the AND gate 133, the other input of which receives the signal R_{B}-. The output of the AND gate 133 is the read/write signal RW, which is fed to the bus scheduler 67.

The signal R_{B}- is also fed via the inverter 134 into the latch 106, the output of which is fed into one input of the AND gate 135. The other input of the AND gate 135 receives R_{B}-. The output of the AND gate 135, the signal R_{END} (Figure 17A), is also fed to the bus scheduler 67. The signals RW and R_{END} enable writing to and reading from the memory page controlled by the controller, and whose page address is indicated by memory write address MWA and the memory read address MRA shown in Figure 16.

In the second converter 91 shown in Figure 15, the write enable signal W_{EN}- is generated by the R/S flip-flop 120, which is set by receiving the signal W_{ST}, which indicates the start of decoding, and is reset by the signal R_{END} from the first converter 90. The D-type flip-flops 121, 122, 123 provide a timing reconciling function, to prevent writing until after reading is completed such that writing is executed when W_{EN}- is low. Writing to a specific page is enabled when the signal Wr_{IorP}- is low or W_{B}- for that page is low. In the manner just described, writing and reading for 2-3 pull-down conversion are controlled.

The circuits described control writing to and reading from the pages M0 to M3 of the frame memory 45, as shown in Figure 16.

Figure 16 illustrates how reconstructed pictures are stored in pages of the frame memory 45, and how they are read out from the respective pages of the frame memory 45 to provide the frames of a non-interlaced digital output signal with a frame rate of 60 Hz. In figure 16, the I-picture I0, indicated by the solid arrow I0, is written into page M0 of the frame memory 45; then, the B-picture B1, indicated by the solid arrow B1, is written into page M2 of the frame memory 45. Next, the following B-picture B2, indicated by the solid arrow B2, is written into page M3 of the frame memory 45, and at the same time, the B-picture B1 is read out twice from page M2 of the frame memory 45, as indicated by the four broken arrows B1. The lines of the odd field and of the even field stored in the page M3 are alternately read out to provide one frame of the digital output signal. Then, the of the odd field and of the even field stored in the page M3 are alternately read a second time to provide the next frame of the digital output signal.

Next, the P-picture P3, indicated by the solid arrow P3, is written into page M1 of the frame memory 45, and, at the same time, the B-picture B2 is read out three times from page M3 of the frame memory 45, as indicated by the six broken arrows B2. The lines of the odd field and of the even field stored in the page M1 are alternately read out to provide one frame of the digital output signal. Then, the lines of the odd field and of the even field stored in the page M1 are alternately read a second time to provide the next frame of the digital output signal. Finally, the lines of the odd field and of the even field stored in the page M1 are alternately read a third time to provide the next frame of the digital output signal.

The page of the frame memory 45 from which the picture B2 is read out is indicated by the memory read address MRA(3). That the picture B2 is read out three times is indicated by the underline under the memory read address. The timing of reading the B-picture B2 is such that the third reading of the picture B2 occurs at the same time as the first half of the B-picture B4 is being written into the page M2, as indicated by the solid line B4. When the second half of the B-picture B4 is being written into page M2 of the frame memory 45, the I-picture I0 is read out twice from page M0 of the frame memory 45, as indicated by the four broken arrows I0. The lines of the odd field and of the even field stored in the page M0 are alternately read out to provide one frame of the digital output signal. This occurs at the same time as second part of the B-picture B4 is being written into the page M2 of the frame memory 45. Then, the lines of the odd field and of the even field stored in the page M0 are alternately read a second time to provide the next frame of the digital output signal. Because, for example, the reading of the I-picture I0 starts half-way through writing the B-picture B4, the timing of the memory read addresses MRA and the memory write addresses MWA shown in Figure 16 do not always coincide.

The B-picture B5, indicated by the solid line B5, is written into page M3 of the frame memory 45. The

first half of the B-picture B5 is written at the same time as the second reading of the I-picture I0 from page M0 of the frame memory. The second half of the B-picture B5 is written into page M3 of the frame memory at the same time as the first of three readings of the B-picture B4 from page M2 of the frame memory 45.

By a process similar to that just described, in which each reconstructed picture is written into one page of the frame memory 45 once at a frame rate of 24 Hz, and in which consecutive frames of the non-interlaced digital output signal are read from a page of the frame memory either twice or three times the remaining pictures in the picture sequence are processed to provide the non-interlaced digital output signal with a frame rate of 60 Hz by 2-3 pull-down conversion.

When the digital output signal is to be an interlaced signal the reading sequence is as shown in Figure 18. The order of reading the fields from each page of the frame memory 45 is controlled by the field order signal FO. When the field order signal FO is low, the odd field is read first, followed by the even field. When the field order signal FO is high, the even field is read first, followed by the odd field. The field order signal FO pulse is generated in the first converters 90A through 90D (Figure 13). In the first converter 90B shown as an example in Figure 14, the field order signal FO is generated from the edges of the 2/3- signal by the D-type flip-flops 110 and 109 (Figure 17I).

In the sequence shown in Figure 18, frames designated by the 2/3-signal are read a second time to provide the required the required field rate. In figure 18, the memory read address MRA of those pages of the frame memory from a field is read twice are designated by an underline. The field order signal FO changes state after each field that is read for a second time.

Figure 18 illustrates how reconstructed pictures are stored in pages of the frame memory 45, and how they are read out from the respective pages of the frame memory 45 to provide the frames of an interlaced digital output signal with a frame rate of 30 Hz. In figure 18, the I-picture I0, indicated by the solid arrow I0, is written into page M0 of the frame memory 45; then, the B-picture B1, indicated by the solid arrow B1, is written into page M2 of the frame memory 45. Next, the following B-picture B2, indicated by the solid arrow B2, is written into page M3 of the frame memory 45, and at the same time, the odd field followed by the event field of the B-picture B1 are read out from page M2 of the frame memory 45, as indicated by the two broken arrows B1. Each field is read out in 1/60 sec.

Next, the P-picture P3, indicated by the solid arrow P3, is written into page M1 of the frame memory 45, and, at the same time, the odd field followed by the even field of the B-picture B2 are read out from page M3 of the frame memory 45. The odd field of the B-picture B2 is then read out from page M3 of the frame memory a second time. This is indicated by the three broken arrows B2. The field order signal FO changes state while the B-picture B2 is being read out so that when the next picture is read out of the frame memory 45, its even field will be read out first.

The timing of reading the B-picture B2 is such that the second reading of the odd field of the picture B2 occurs at the same time as the first half of the B-picture B4 is being written into the page M2, as indicated by the solid line B4. When the second half of the B-picture B4 is being written into page M2 of the frame memory 45, the even field followed by the odd field of the I-picture I0 is read out from page M0 of the frame memory 45, as indicated by the two broken arrows I0, in response to the changed state of the field order signal FO. The second odd field of B-picture B2 and the even field of I-picture I0 form the next frame of the interlaced digital output signal.

The B-picture B5, indicated by the solid line B5, is written into page M3 of the frame memory 45. The first half of the B-picture B5 is written at the same time as the odd field of the I-picture I0 is read out from page M0 of the frame memory. The second half of the B-picture B5 is written into page M3 of the frame memory at the same time as the even field of the B-picture B4 is read out from page M2 of the frame memory 45 a first time.

The P-picture P6, indicated by the solid line P6, is then written in to page M0 of the frame memory 45, and, at the same time, the odd field of the B-picture B4 is read out from page M2 of the frame memory 45, followed by the even field of the B-picture B4, read for a second time. The odd field of I-picture I0 and the even field of B-picture B4 (first reading) form one frame of the interlaced digital output signal, as do the odd field and the even field (second reading) of the B-picture B4. The state of the field order signal FO changes state in the course of reading the B-picture B4 so that the next picture to be read, B5, will be read with its odd field first.

By a process similar to that just described, in which each reconstructed picture is written into one page of the frame memory 45 once at a frame rate of 24 Hz, and in which consecutive frames of the non-interlaced digital output signal are read from a page of the frame memory either twice or three times the remaining pictures in the picture sequence are processed to provide the non-interlaced digital output signal with a frame rate of 60 Hz by 2-3 pull-down conversion.

In the system described above frames of the video signal may be coded in field mode, in which frames consisting of fields derived from two consecutive frames of the motion picture film source may be coded as two fields to improve the compression efficiency. Moreover, the decoder according to the invention

provides 2-3 pull-down conversion using no more pages of frame memory than are required for decoding, thus providing a simplified construction in which additional pages of frame memory are not required.

Further, in the decoder according to the invention will provide an interlaced digital output signal or a non-interlaced digital output signal simply by controlling the addressing by which the reconstructed pictures stored in the frame memory are read out to provide the digital output signal, during which 2-3 pull-down conversion is also carried out. Hence, both scan mode conversion and 2-3 pull-down conversion may be implemented by the same control circuits in a reproducing apparatus in which a compressed digital video signal derived from motion picture film source and having a frame rate of 24 Hz is decoded and subject to 2-3 pull down conversion by means of a simple circuit construction, to provide either an interlaced or a non-interlaced video signal.

Furthermore, the reproducing apparatus including the decoder according to the invention will reproduce a compressed digital video signal derive from a motion film source such as a motion picture film, and the video output signal from the apparatus may be connected, as desired, to interlaced or non-interlaced television monitors for display. Video signals derived from motion picture film sources may be included in a so-called multi-media environment, and the video signal resulting from decoding by the decoder according to the invention may be displayed on computer monitors at home or in the office, greatly improving the useability of such systems.

It should be noted that, while the decoding apparatus according to the invention has been described with reference to reproducing and decoding a compressed video signal recorded on an optical disk as the recording medium, the invention is not limited to this, and may be applied to decoding compressed video signals recorded on magnetic tape or other recording media. Moreover, the decoder according to the invention may also be used for decoding compressed video signals received via a transmission or distribution system such as broadcast television, cable television, telephone, ISDN network, computer network, etc.

It should also be noted that the decoder according to the invention can also be used to apply 2-3 pull-down conversion to derive an interlaced or a non-interlaced video signal with a field rate or a frame rate, respectively, of 50 Hz from the compressed video signal having a frame rate of 24 Hz. To effect such 2-3 pull-down conversion, the decoder 101 is reprogrammed to generate the 2/3- signal once every twelve frames written into the frame memory 45 instead of once every two frames as in the 60 Hz version.

While there has been described in connection with the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications may be aimed, therefore, to cover in the appended claims all such changes and modifications as fall within the true spirit and scope of the invention.

Claims

1. An apparatus for expanding a compressed digital video signal representing a motion picture to provide a digital video output signal, the compressed digital video signal comprising plural interlaced frames and having a frame rate of 24 Hz, the digital video output signal comprising plural pictures and having a picture rate of at least 49 Hz, the apparatus comprising:

   a frame memory (45) comprising no more than four pages, each page storing one frame;

   expander means for expanding each frame of the compressed digital video signal to derive a reconstructed interlaced frame; and

   control means (68) for controlling:

   writing of each reconstructed interlaced frame into one page of the frame memory (45), and

   reading out of the reconstructed interlaced frames stored in the pages of the frame memory (45) to provide the pictures of the digital video output signal, the reading out being controlled to effect 2-3 pull down conversion of the reconstructed interlaced frames stored in the pages of the frame memory (45) with a frame rate of 24 Hz to provide the pictures of the digital video output signal with a picture rate of at least 49 Hz.

2. The apparatus of claim 1, wherein:

   the digital video output signal is interlaced, and each picture thereof is one field; and

   the control means (68) controls the reading out of the reconstructed interlaced frames stored in the pages of the frame memory (45) to read out each reconstructed interlaced frame to provide at least two fields of the digital video output signal.

3. The apparatus of claim 2, wherein:

   the digital video output signal has a field rate of 50 Hz; and

   the control means (68) controls the reading out of the reconstruced interlaced frames stored in the pages of the frame memory (45) to read out eleven consecutive reconstructed interlaced frames to provide two fields of the digital video output signal, and to read out a twelth reconstructed interlaced frame to provide three fields of the digital video output signal.

4. The apparatus of claim 2, wherein:
the digital video output signal has a field rate of 60 Hz; and
the control means (68) controls the reading out of the reconstructed interlaced frames stored in the pages of the frame memory (45) to read out consecutive reconstructed interlaced frames to provide alternately two fields and three fields of the digital video output signal.

5. The apparatus of any of claims 1 to 4, wherein:
the digital video output signal is non-interlaced signal, and each picture thereof is one frame:
each reconstructed interlaced frame stored in one page of the frame memory (45) includes and odd field and an even field, each field including plural lines; and
the control means (68) controls the reading out of the interlaced reconstructed frames stored in the pages of the frame memory (45) such that each reconstructed interlaced frame is read out at least twice, and lines of the odd field thereof are read out alternately with the lines of the even field thereof to provide one picture of the digital video output signal.

6. The apparatus of claim 5, wherein:
the digital video output signal has a field rate of 50 Hz; and
the control means (68) controls the reading out of the reconstructed interlaced frames stored in the pages of the frame memory (45) to read out eleven consecutive reconstructed interlaced frames to provide two frames of the digital video output signal, and to read out a twelfth reconstructed interlaced frame to provide three frames of the digital video output signal.

7. The apparatus of claim 5, wherein:
the digital video output signal has a field rate of 60 Hz; and
the control means (68) controls the reading of the reconstructed interlaced frames stored in the pages of the frame memory (45) to read out consecutive reconstructed interlaced frames to provide alternately two frames and three frames of the digital video output signal.

8. The apparatus of any of claims 1 to 7, wherein:
the control means (68) is additionally for reading out a selected reconstructed interlaced frame as a read-out reconstructed interlaced frame; and
the expander means includes:
motion compensation means (46) for deriving a reference picture from the readout reconstructed interlaced frame, and
means for reconstructing a reconstructed interlaced frame from the reference picture and a frame of the compressed digital video signal.

9. The apparatus of claim 8, wherein:
the compressed digital video signal includes a motion vector;
the apparatus additionally comprises means for extracting the motion vector from the compressed digital video signal; and
the motion compensation means (46) derives the reference picture from the read out reconstructed interlaced frame in response to the motion vector extracted from the compressed digital video signal.

10. The apparatus of any of claims 1 to 9, wherein:
a reconstructed interlaced frame is written into one of the pages of the frame memory (45) in response to a write mode signal for the one of the pages;
a picture of the digital video output signal is read out of the one of the pages of the frame memory (45) in response to a read mode signal for the one of the pages; and
the control means (68) comprises:
first converter means (90A-90D) for:
generating the write mode signal for one page of the frame memory (45) when a reconstructed frame provided by the expander means is to be written into the one page of the frame memory; and
generating the read mode signal when the reconstructed frame stored in the one page of the frame memory (45) is to be read out to provide a picture of the digital video output signal, and
second converter means (91A-91D) for controlling timing of generating the write mode signal and the read mode signal for the one page of the frame memory (45).

11. The apparatus of claim 10, wherein the first converter means (90A-90D) is for generating the read mode signal to control a number of times the reconstructed interlaced frame is read out from the one page of the frame memory (45).

12. The apparatus of claim 10, wherein the first converter means (90A-90D) is additionally for generating a signal to read out the reconstructed field from the one page of the frame memory (45) as at least two fields.

13. A system for compressing a digital video input signal representing a motion picture to provide a compressed digital video signal comprising plural

interlaced frames and having a frame rate of 24 Hz, and for expanding the compressed digital video signal to provide a digital video output signal comprising plural pictures having a picture rate of at least 49 Hz, the system comprising:

an encoder (4), including

means for deriving from a motion picture film source a non-interlaced digital video signal comprising plural frames having a frame rate of 24 Hz,

means for performing 2-3 pull-down conversion of the non-interlaced digital video signal to derive an interlaced digital video signal having a frame rate of greater than 24 Hz,

compressor means for compressing the interlaced digital video signal to provide a compressed digital video signal with a frame rate of greater than 24 Hz, and

means for reducing the frame rate of the compressed digital video signal with a frame rate of greater than 24 Hz to 24 Hz to provide the compressed digital video signal; and

a decoder (11), including:

a frame memory (45) comprising no more than four pages, each page storing one frame,

expander means (66) for expanding the compressed digital signal to derive a reconstructed interlaced frame from each frame of the compressed digital video signal,

control means (68) for controlling:

writing of each reconstructed interlaced frame into one page of the frame memory (45); and

reading of the reconstructed interlaced frames stored in the four pages of the frame memory (45) to provide pictures of the digital video output signal, the reading out being controlled to effect 2-3 pull down conversion of the reconstructed interlaced frames stored in the frame memory (45) with a frame rate of 24 Hz to provide the pictures of the digital video output signal with a picture rate of at least 49 Hz.

14. The system of claim 13, wherein:

the digital video output signal is interlaced, and each picture thereof is one field; and

in the decoder (11), the control means (68) controls the reading out of the reconstructed interlaced frames stored in the pages of the frame memory (45) to read out each reconstructed interlaced frame to provide at least fields of the digital video output signal.

15. The system of claims 13 or 14, wherein:

the digital video output signal is non-interlaced, and each picture thereof is one frame; and

in the decoder (11):

each reconstructed interlaced frame stored in one page of the frame memory (45) includes an odd field and an even field, each field including plural lines, and

the control means (68) controls the reading out of the interlaced reconstructed frames stored in the pages of the frame memory (45) such that each reconstructed interlaced frame is read out at least twice, and lines of the odd field thereof are read out alternately with the lines of the even field thereof to provide one picture of the digital video output signal.

16. The system of any of claims 13 to 15,wherein, in the decoder (11):

the control means (68) is additionally for reading out a selected reconstructed interlaced frame as a read-out reconstructed interlaced frame; and

the expander means includes:

motion compensation means for deriving a reference picture from the read-out reconstructed interlaced frame, and

means for reconstructing a reconstructed interlaced frame from the reference picture and a frame of the compressed digital video signal.

17. The system of claim 16, wherein:

in the encoder (4), the compressor means includes means for generating a motion vector and for including the motion vector in the compressed digital video signal;

the decoder (11) additionally comprises means for extracting the motion vector from the compressed digital video signal; and

in the decoder (11), the motion compensation means derives the reference picture from the read out reconstructed interlaced frame in response to the motion vector extracted from the compressed digital video signal.

18. The system of any of claims 13 to 17, wherein, in the decoder (11):

a reconstructed interlaced frame is written into one of the pages of the frame memory (45) in response to a write mode signal for the one of the pages;

a picture of the digital video output signal is read out of the one of the pages of the frame memory (45) in response to a read mode signal for the one of the pages; and

the control means (68) comprises:

first converter means for:

generating the write mode signal for one page of the frame memory (45) when a reconstructed frame provided by the expander means is to be written into the one page of the

frame memory; and

generating the read mode signal when the reconstructed frame stored in the one page of the frame memory (45) is to be read out to provide a picture of the digital video output signal, and

second converter means for controlling timing of generating the write mode signal and the read mode signal for the one page of the frame memory (45).

19. A method of using a frame memory (45) comprising no more than four pages, each page storing one frame, to expand a compressed digital video signal representing a motion picture to provide a digital video output signal, the compressed digital video signal comprising plural interlaced frames and having a frame rate of 24 Hz, the digital video output signal comprising plural pictures and having a picture rate of at least 49 Hz, the method comprising the steps of:

expanding each frame of the compressed digital video signal to derive a reconstructed interlaced frame;

writing each reconstructed interlaced frame into one page of the frame memory (45);

reading out the reconstructed interlaced frames written in the pages of the frame memory (45) to provide the pictures of the digital video output signal; and

selecting the page of the frame memory (45) whereinto each reconstructed interlaced frame is written, and the page wherefrom a reconstructed interlaced frame is read out to provide each picture of the digital video output signal, and additionally selecting a number of times each reconstructed interlaced frame is read out to effect 2-3 pull down conversion of the reconstructed interlaced frames written in the pages of the frame memory (45) with a frame rate of 24 Hz to provide the pictures of the digital video output signal with a picture rate of at least 49 Hz.

20. The method of claim 19, wherein:

the digital video output signal is interlaced, and each picture thereof is one field;

in the step of writing each reconstructed interlaced frame into one page of the frame memory (45), each reconstructed frame is written as and odd field and an even field;

in the step of selecting the number of times each reconstructed interlaced frames is read out, the number of times each reconstructed interlaced frame is read out is selected to be at least one; and

in the step of reading out the reconstructed interlaced frames, the odd field and the even field of the reconstructed interlaced frame are read out to provide at least two fields of the digital video output signal.

21. The method of claims 19 or 20, wherein:

the digital video output signal is non-interlaced, and each picture thereof is one frame;

in the step of writing each reconstructed interlaced frame into one page of the frame memory (45), each reconstructed frame is written as and odd field and an even field, each field including plural lines;

in the step of selecting the number of times each reconstructed interlaced frames is read out, the number of times each reconstructed interlaced frame is read out is selected to be at least two so that each reconstructed interlaced frame is read out to provide at least two frames of the digital video output signal; and

in the step of reading out the reconstructed interlaced frames, the lines of the odd field of each reconstructed interlaced frame are read alternately with the lines of the even field thereof to provide one picture of the digital video output signal.

22. The method of any of claims 19 to 21, wherein:

the method additionally comprises the step of reading out a selected reconstructed interlaced frame as a read-out reconstructed interlaced frame; and

the step of expanding the compressed digital signal includes the steps of:

deriving a reference picture from the read-out reconstructed interlaced frame, and

reconstructing a reconstructed interlaced frame from the reference picture and a frame of the compressed digital video signal.

23. The method of claim 22, wherein:

the compressed digital video signal includes a motion vector;

the method additionally comprises the step of extracting the motion vector from the compressed digital video signal; and

in the deriving a reference picture from the read-out reconstructed interlaced frame, the reference picture is derived from the read out reconstructed interlaced frame in response to the motion vector extracted from the compressed digital video signal.

24. The method of claim 19, wherein:

in the step of writing each reconstructed interlaced frame, the reconstructed interlaced frame is written into one of the pages of the frame memory (45) in response to a write mode signal for the one of the pages;

in the step of reading out the reconstruct-

ed interlaced frames, a picture of the digital video output signal is read out of one of the pages of the frame memory (45) in response to read mode signal for the one of the pages; and

the selecting step comprises the steps of:

generating the write mode signal for one page of the frame memory (45) when a reconstructed frame provided by the expander means is to be written into the one page of the frame memory (45),

generating the read mode signal when the reconstructed frame stored in the one page of the frame memory (45) is to be read out to provide a picture of the digital video output signal, and

controlling timing of generating the write mode signal and generating the read mode signal for the one page of the frame memory (45).

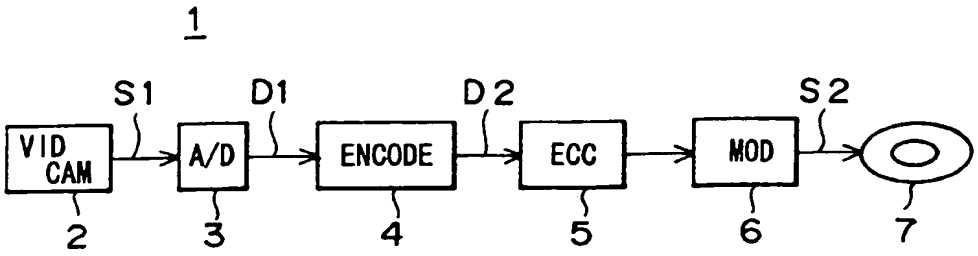
1
S1
D1
D2
S2
VID CAM
A/D
ENCODE
ECC
MOD
2
3
4
5
6
7

FIG. 1

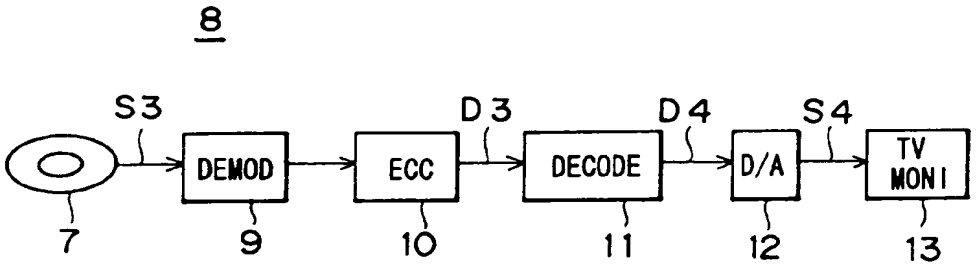
8
S3
D3
D4
S4
DEMOD
ECC
DECODE
D/A
TV MONI
7
9
10
11
12
13

FIG. 2

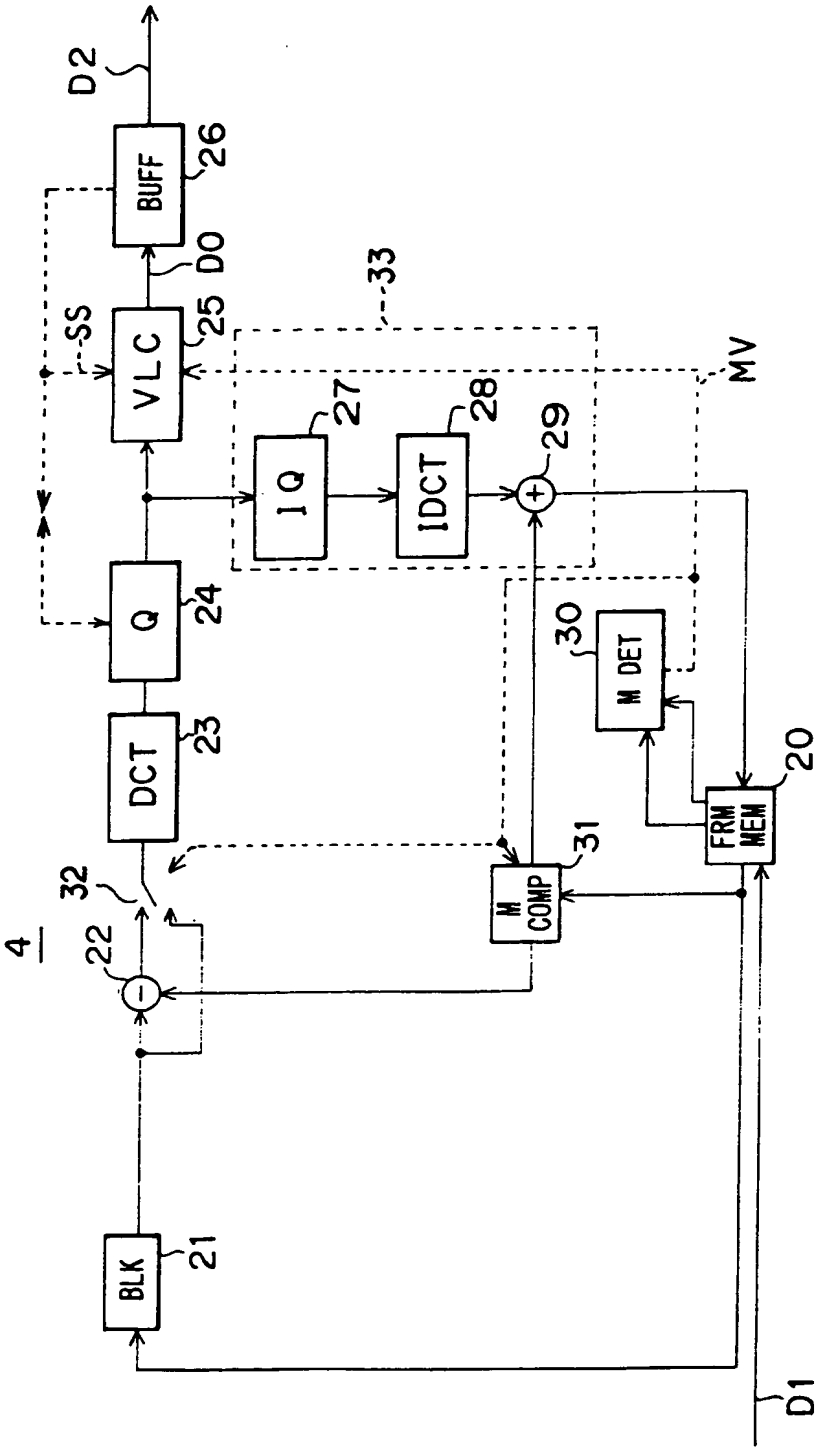
D2
BUFF
26
D0
25
VLC
SS
33
MV
27
IQ
28
IDCT
29
24
Q
30
M DET
23
DCT
20
FRM MEM
31
M COMP
32
4
22
21
BLK
D1

FIG. 3

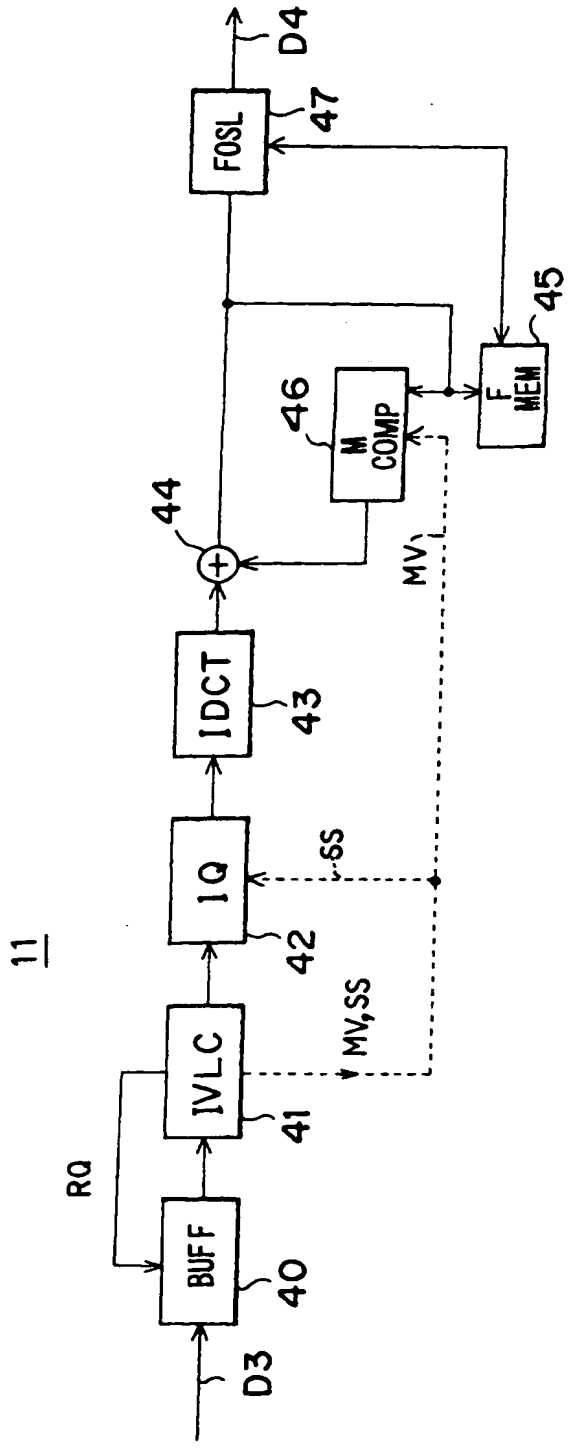
11
D3
BUFF
40
RQ
IVLC
41
MV,SS
IQ
42
SS
IDCT
43
44
MV
M COMP
46
F MEM
45
FOSL
47
D4

FIG. 4

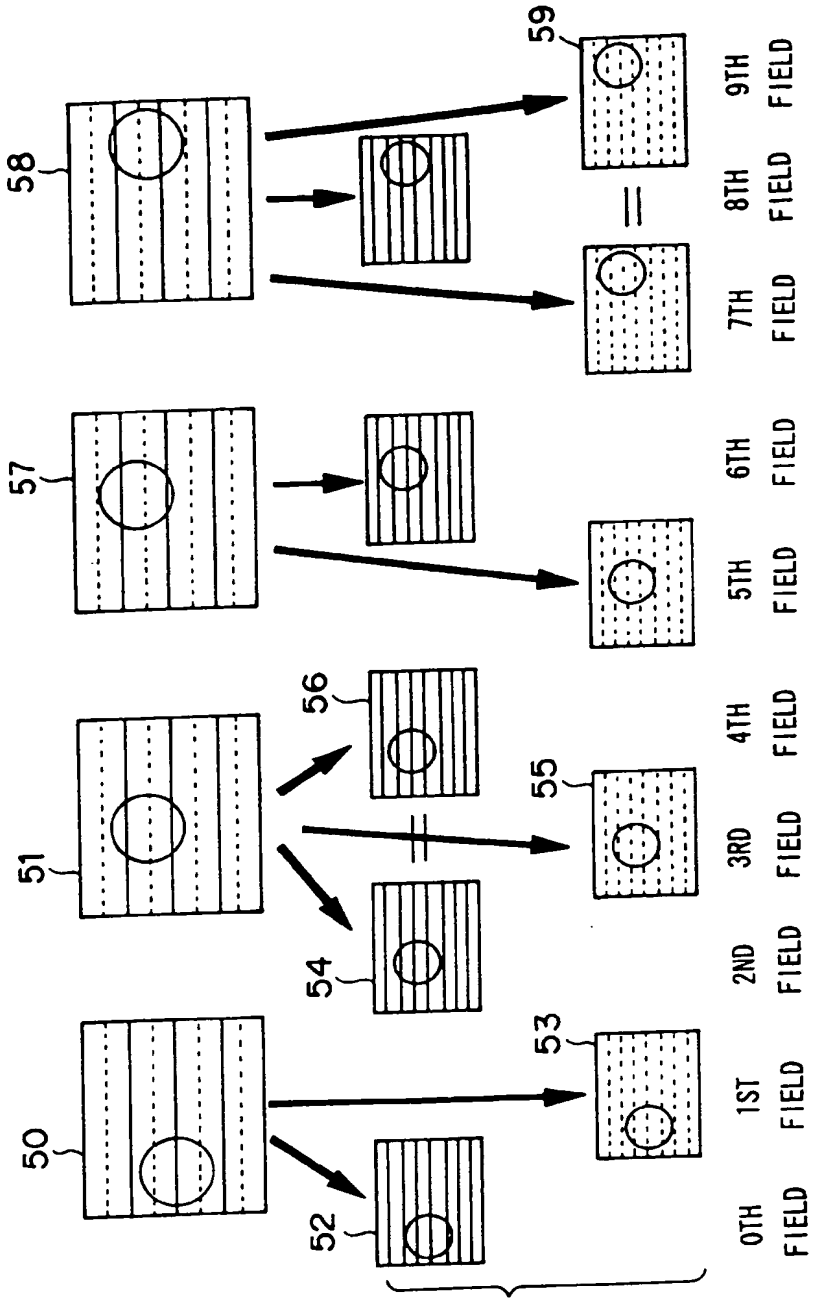
50
51
52
53
54
55
56
57
58
59
0TH FIELD
1ST FIELD
2ND FIELD
3RD FIELD
4TH FIELD
5TH FIELD
6TH FIELD
7TH FIELD
8TH FIELD
9TH FIELD

FIG. 5A

FIG. 5B

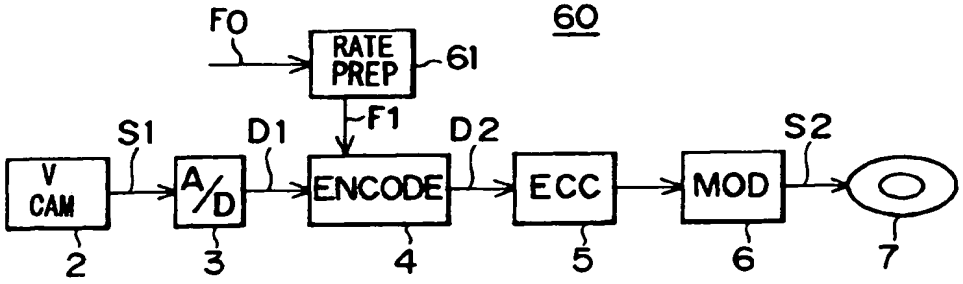
F0
RATE PREP
61
60
F1
S1
D1
D2
S2
V CAM
A/D
ENCODE
ECC
MOD
2
3
4
5
6
7

FIG. 6

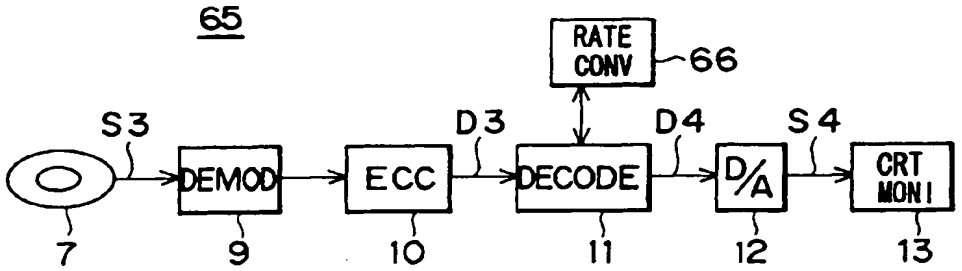
65
RATE CONV
66
S3
D3
D4
S4
DEMOD
ECC
DECODE
D/A
CRT MONI
7
9
10
11
12
13

FIG. 7

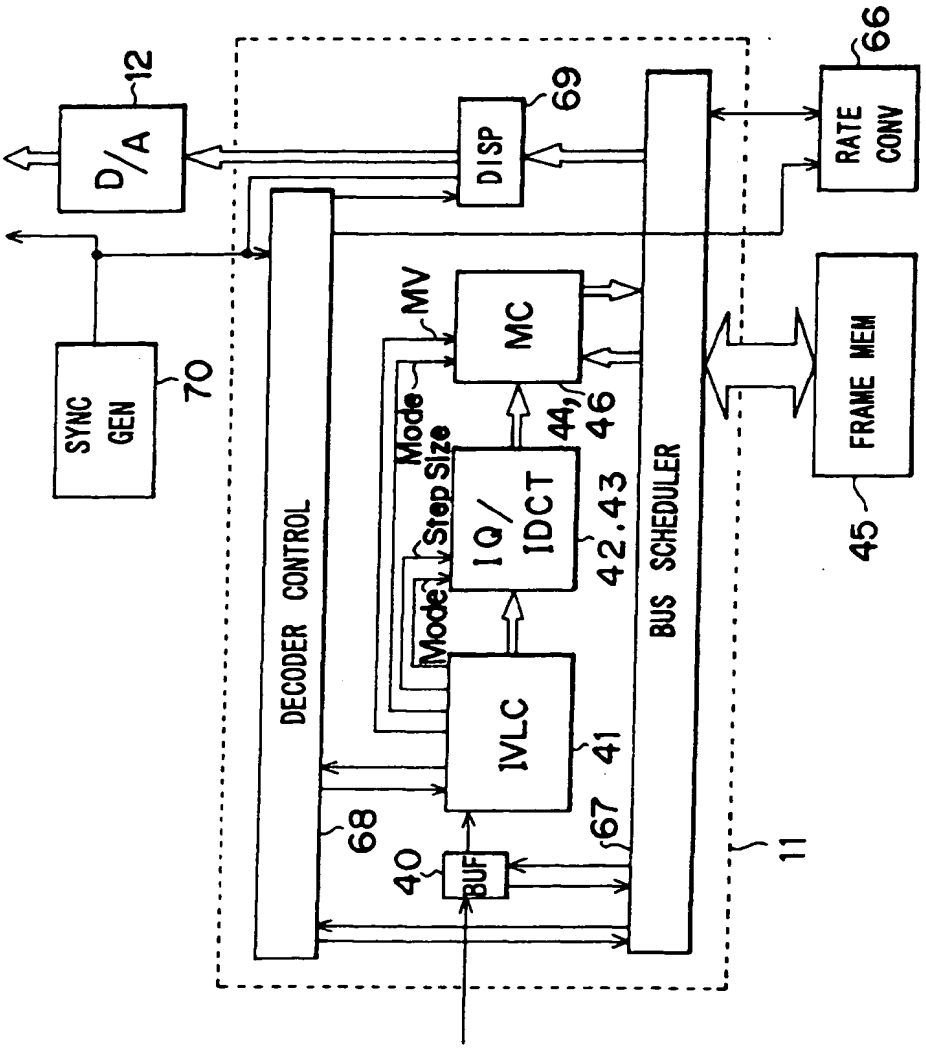
D/A
12
DISP
69
RATE CONV
66
SYNC GEN
70
DECODER CONTROL
MV
MC
Mode
Step Size
44
46
IQ/ IDCT
42.43
FRAME MEM
45
Mode
IVLC
41
BUS SCHEDULER
68
40
BUF
67
11

FIG. 8

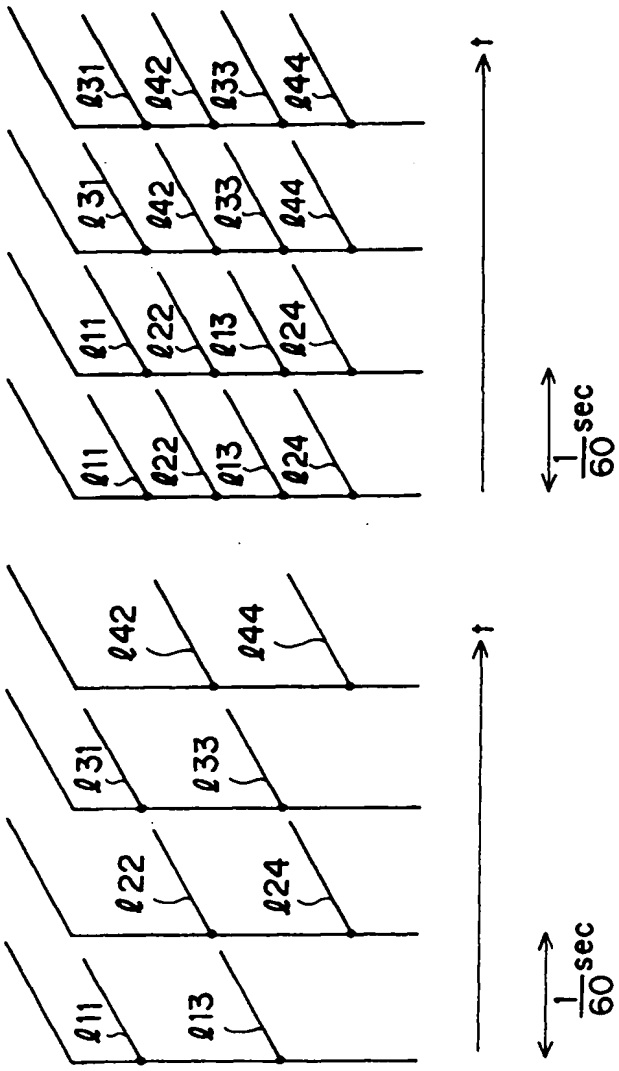
Q11
Q13
Q22
Q24
Q31
Q33
Q42
Q44
t
1/60 sec
Q11
Q22
Q13
Q24
Q31
Q42
Q33
Q44
t
1/60 sec

FIG. 9A

FIG. 9B

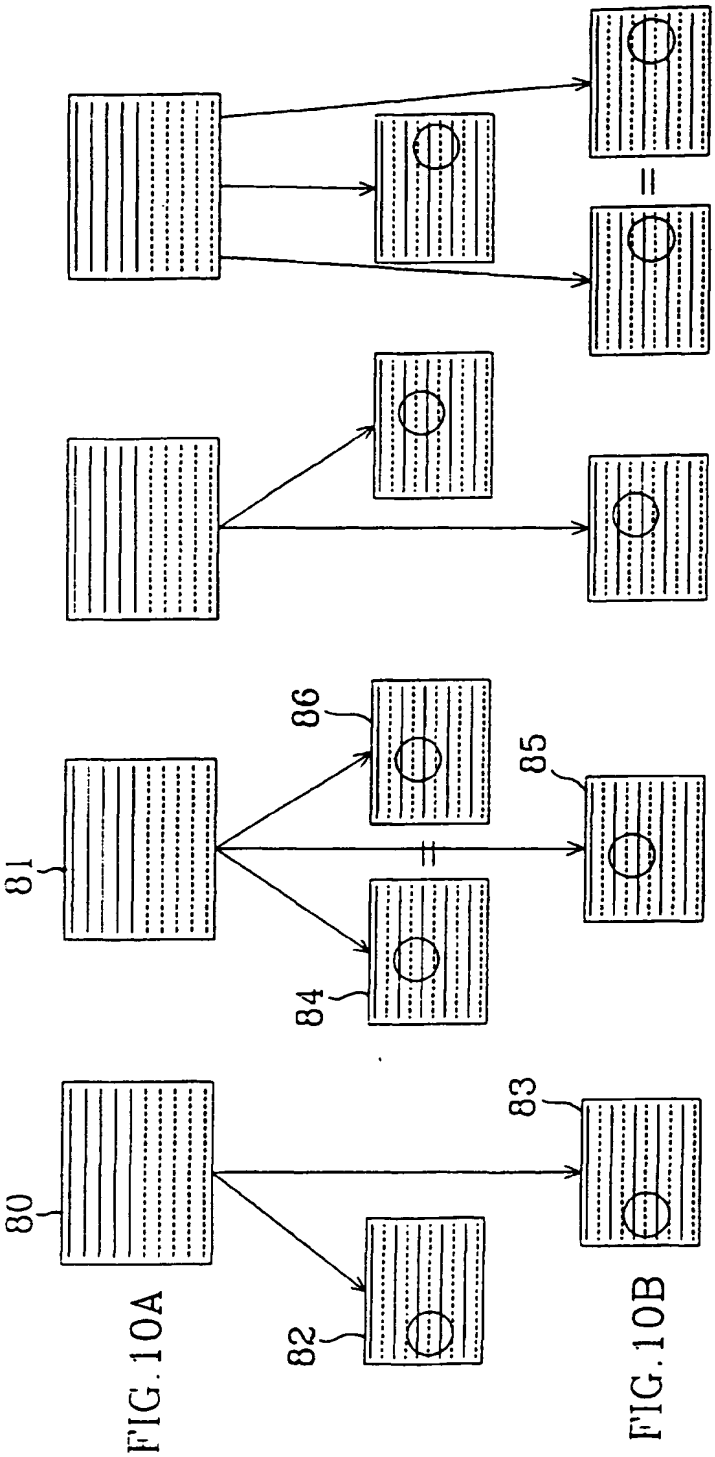

FIG.10A

FIG.10B

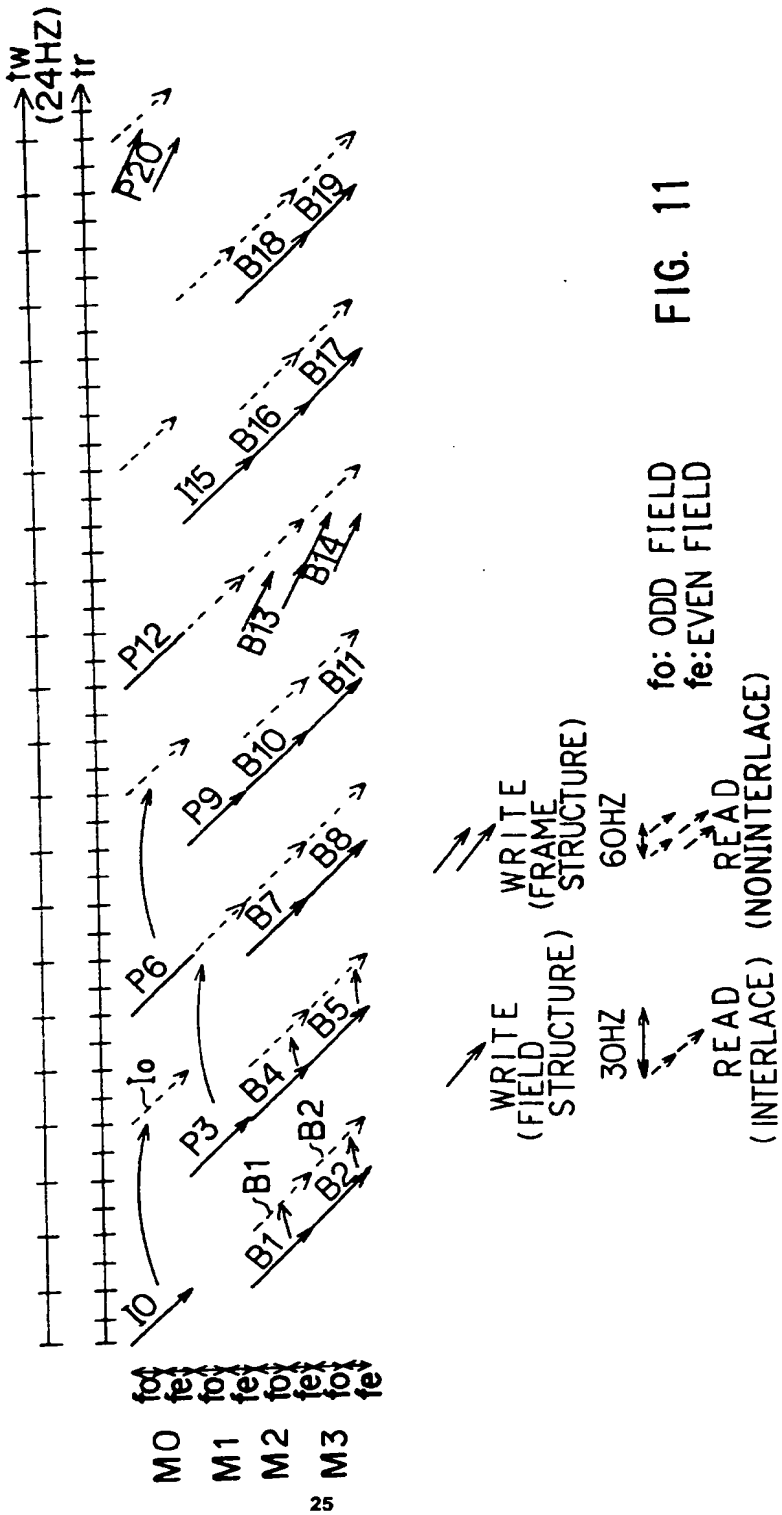
tw
(24HZ)
tr
I0
P3
P6
P9
P12
I15
P20
B1
B1
B2
B2
B4
B5
B7
B8
B10
B11
B13
B14
B16
B17
B18
B19
fo fe fo fe fo fe fo fe
M0 M1 M2 M3
WRITE (FIELD STRUCTURE)
30HZ
READ (INTERLACE)
WRITE (FRAME STRUCTURE)
60HZ
READ (NONINTERLACE)
fo: ODD FIELD
fe: EVEN FIELD

FIG. 11

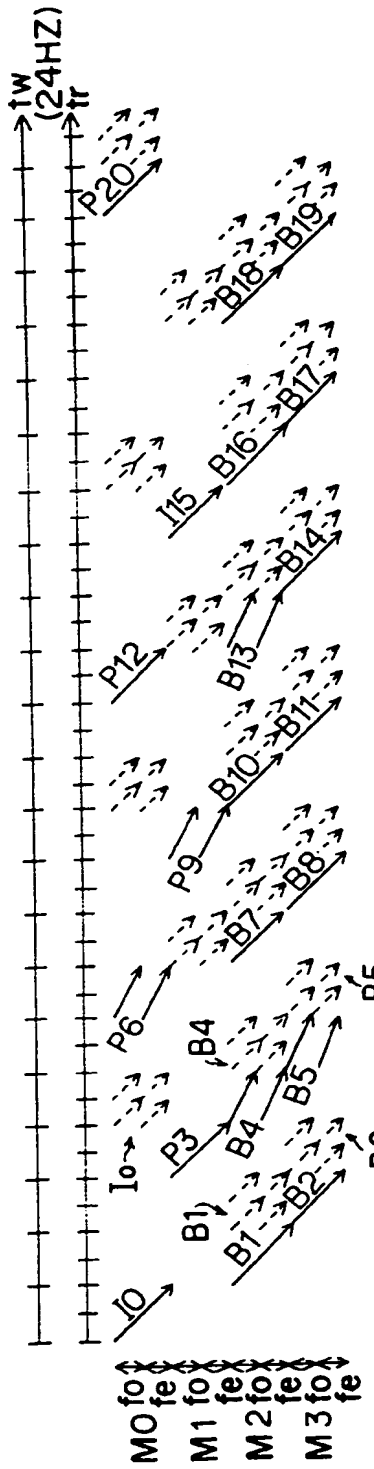
tw
(24HZ)
tr
I0
P20
B18
B19
I15
B16
B17
P12
B13
B14
P9
B10
B11
P6
B7
B8
B4
B5
P3
B4
B5
Io
B1
B2
B1
B2
M0 fo fe
M1 fo fe
M2 fo fe
M3 fo fe

FIG. 12

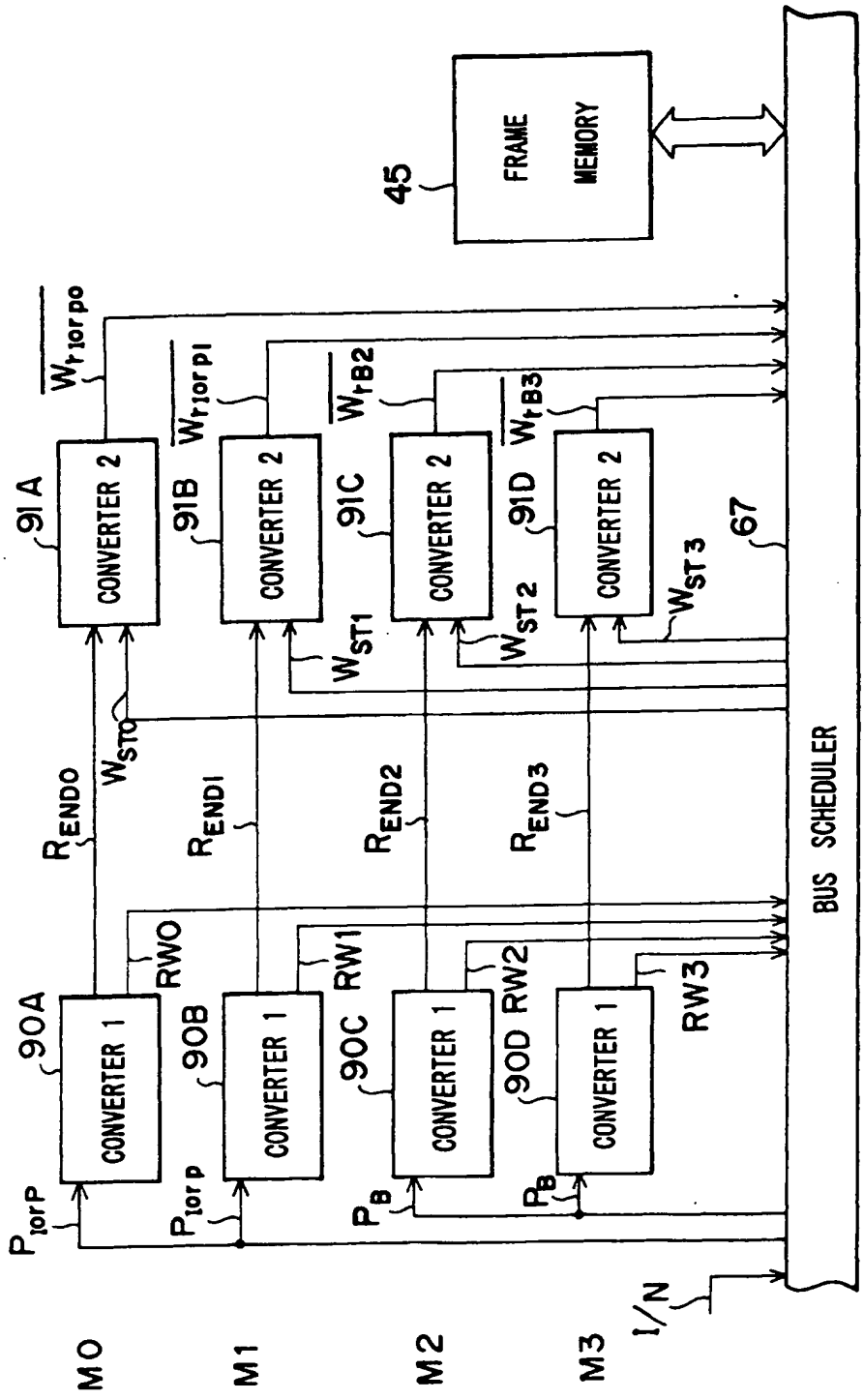
45
FRAME MEMORY
BUS SCHEDULER
67
91A
91B
91C
91D
CONVERTER 2
90A
90B
90C
90D
CONVERTER 1
M0
M1
M2
M3
I/N
RW0
RW1
RW2
RW3
W_{TIORP0}
W_{TIORP1}
W_{TB2}
W_{TB3}
W_{ST0}
W_{ST1}
W_{ST2}
W_{ST3}
R_{END0}
R_{END1}
R_{END2}
R_{END3}
P_{IORP}
P_{IORP}
P_B
P_B

FIG. 13

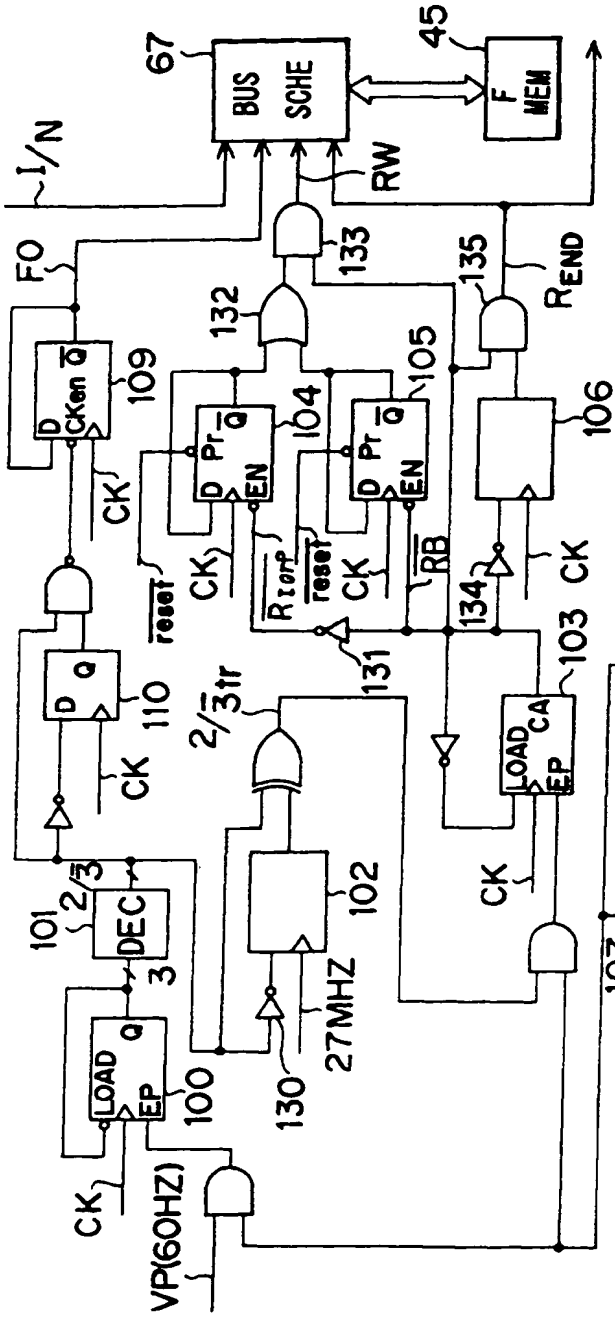
67
BUS SCHE
45
F MEM
I/N
RW
FO
133
135
R_{END}
132
109
105
104
106
CK
reset
RB
134
131
103
110
$2/3_{tr}$
W_{B_END}
108
101
2/3
DEC
3
102
27MHZ
130
100
LOAD
EP
CA
CLR
CKon
VP(24HZ)
107
PSC
VP(60HZ)
GOP
$\overline{W_B}$

FIG. 14

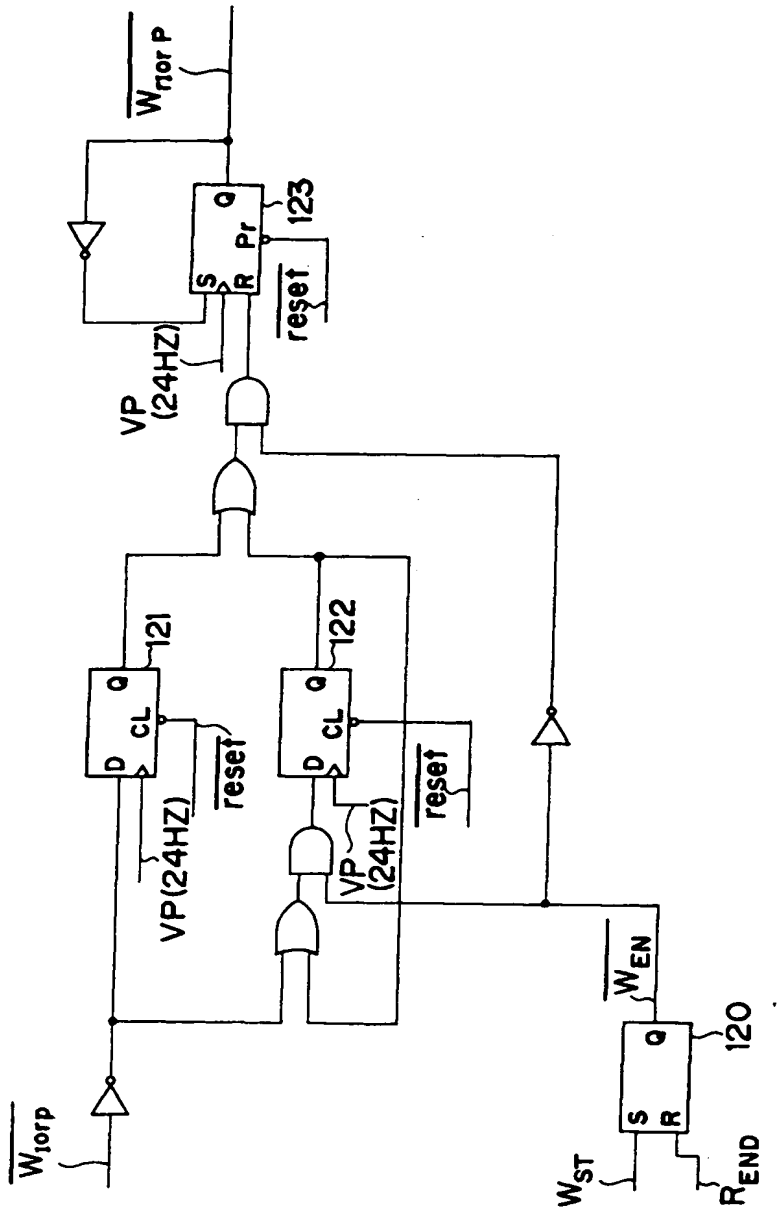
$\overline{W_{norP}}$
Q
Pr
123
S
R
reset
VP (24HZ)
121
122
D
CL
reset
VP(24HZ)
reset
VP (24HZ)
$\overline{W_{EN}}$
120
$\overline{W_{norp}}$
W_{ST}
R_{END}

FIG. 15

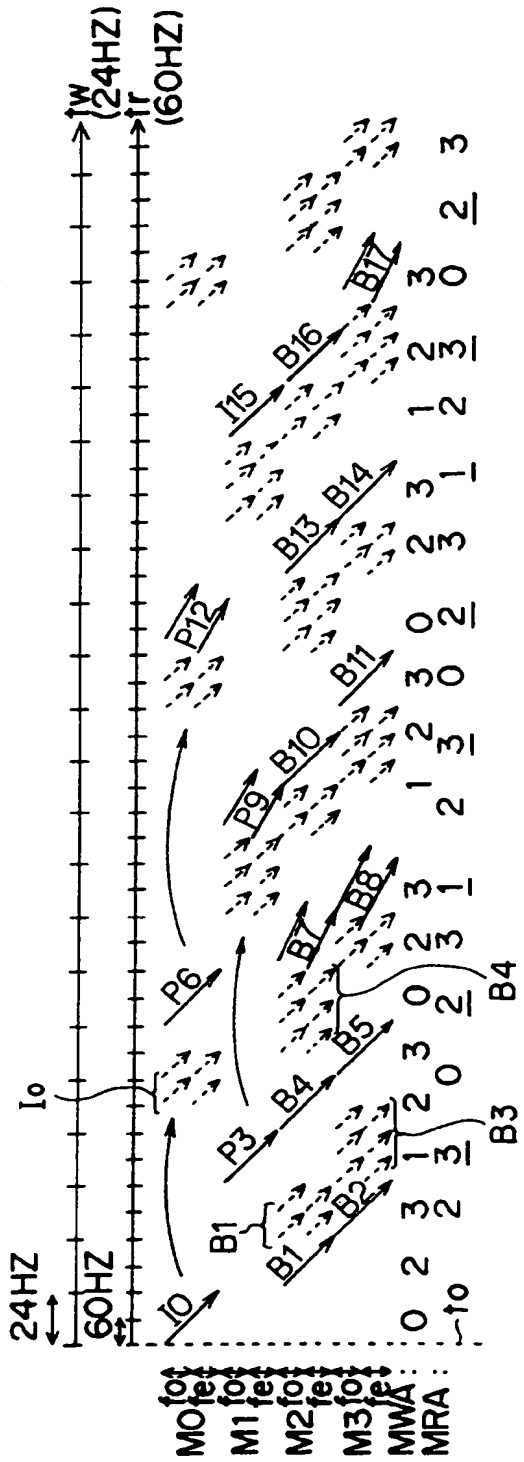
W (24HZ)
r (60HZ)
24HZ
60HZ
I0
Io
P3
P6
P9
P12
I15
B1
B2
B3
B4
B5
B7
B8
B10
B11
B13
B14
B16
B17
M0
M1
M2
M3
MWA
MRA

FIG. 16

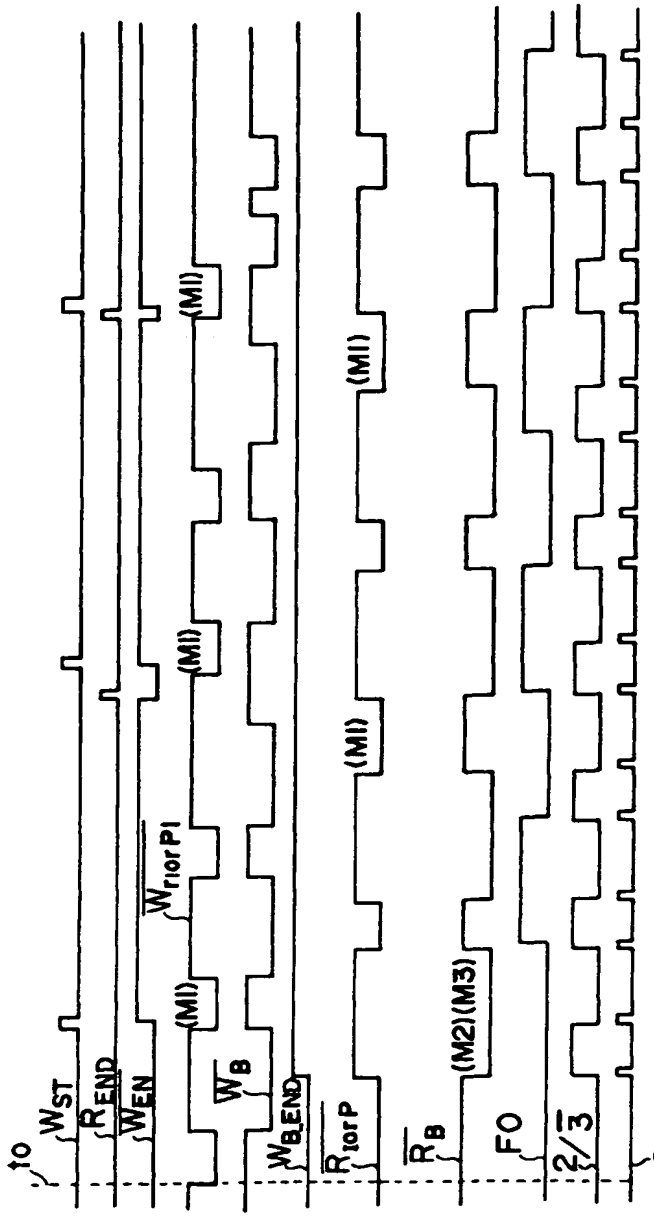

FIG. 17A
FIG. 17B
FIG. 17C
FIG. 17D
FIG. 17E
FIG. 17F
FIG. 17G
FIG. 17H
FIG. 17I
FIG. 17J
FIG. 17K

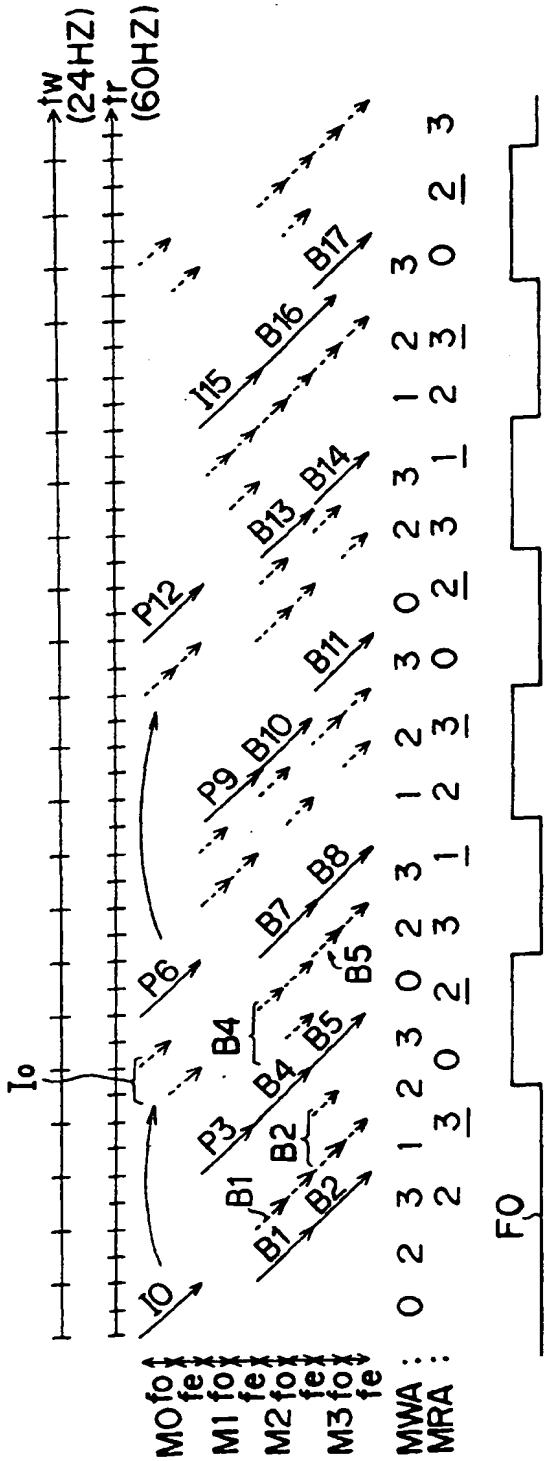
tw (24HZ)
tr (60HZ)
I0
I15
P12
P9
P6
P3
B17
B16
B14
B13
B11
B10
B8
B7
B5
B4
B2
B1
MWA :: 0 2 3 1 2 3 0 2 3 1 2 3 0 2 3 1 2 3 0 2 3
MRA :: 2 3 0 2 3 1 2 3 0 2 3 1 2 3 0 2 3 1
F0
M0 fo fe
M1 fo fe
M2 fo fe
M3 fo fe

FIG. 18